General Description

BDE-BW20C is a dual-processor low power IoT network gateway module integrates multiple wireless technologies and protocols which include 2.4GHz and 5GHz Dual-Band Wi-Fi 802.11a/b/g/n, Bluetooth 5.2 Low Energy, BLE mesh, Thread, Zigbee, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), Wi-SUN, proprietary systems, SimpleLink TI 15.4-Stack (2.4 GHz) and Dynamic Multiprotocol Manager (DMM) driver. The module combines a low power Dual-Band Wi-Fi SoC CC3235SF and a 2.4GHz low power multiprotocol wireless SoC CC2652P with all external components including a Dual-band chip antenna. Both SoCs are integrated with an Arm® Cortex®-M4 application MCU and are able to run independently with Wi-Fi/BLE Coexistence design.

Key Features

- Wi-Fi Dual band 2.4GHz and 5GHz, 802.11a/b/g/n
- BLE5.2, Thread, Zigbee®, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), Wi-SUN®, proprietary systems, SimpleLink™ TI 15.4-Stack (2.4 GHz), Dynamic Multiprotocol Manager (DMM).
- Wi-Fi – BLE Coexistence (2.4GHz).
- Industrial temperature: –40°C to +85°C
- Dimension: 29mm x 29mm x 2.4mm
- Antenna: Integrated Dual-band chip antenna or UFL connector
- FCC, IC, CE-REC compliant

Wi-Fi core Features

- 802.11a/b/g/n: 2.4 GHz and 5 GHz
- FIPS 140-2 Level 1 validated IC inside
- Multilayered security features help developers protect identities, data, and software IP
- Low-power modes for battery-powered applications
- Coexistence with 2.4-GHz radios
- Transferrable Wi-Fi Alliance® certification
- Application microcontroller subsystem:
  - Arm® Cortex®-M4 core at 80 MHz
  - User-dedicated memory:
    - 256KB of RAM
    - 1MB of executable flash
  - Rich set of peripherals and timers:
    - McASP supports two I2S channels
    - SD, SPI, I2C, UART
    - 8-bit synchronous imager interface
    - 4-channel 12-bit ADCs
    - 4 general-purpose timers (GPT) with 16-bit PWM mode
    - Watchdog timer
    - Up to 27 GPIO pins
    - Debug interfaces: JTAG, cJTAG, SWD
- Wi-Fi network processor subsystem:
  - Wi-Fi® core:
    - 802.11 a/b/g/n 2.4 GHz and 5 GHz
    - Modes:
      - Access point (AP)
      - Station (STA)
      - Wi-Fi Direct® (only supported on 2.4GHz)
    - Security:
      - WEP
      - WPA™/ WPA2™ PSK
      - WPA2 Enterprise
      - WPA3™ Personal
  - Internet and application protocols:
    - HTTPs server, mDNS, DNS-SD, DHCP
    - IPv4 and IPv6 TCP/IP stack
    - 16 BSD sockets (fully secured TLS v1.2 and SSL 3.0)
  - Built-in power management subsystem:
    - Configurable low-power profiles (always on, intermittently connected, tag)
    - Advanced low-power modes
    - Integrated DC/DC regulators
- Multilayered security features:
  - Separate execution environments
  - Networking security
  - Device identity and key
  - Hardware accelerator cryptographic engines (AES, DES, SHA/MD5, CRC)
  - File system security (encryption, authentication, access control)

- Initial secure programming
- Software tamper detection
- Secure boot
- Certificate signing request (CSR)
- Unique per device key pair

- Application throughput
  - UDP: 16 Mbps
  - TCP: 13 Mbps
- Power-Management Subsystem:
  - Integrated DC/DC converters support a wide range of supply voltage:
    - Single wide-voltage supply VBAT: 2.3 V to 3.6 V
  - Advanced low-power modes:
    - Shutdown: 1 µA, Hibernate: 5.5 µA
    - Low-power deep sleep (LPDS): 120 µA
    - Idle connected (MCU in LPDS): 710 µA
    - RX traffic (MCU active): 59 mA
    - TX traffic (MCU active): 223 mA
  - Wi-Fi TX power
    - 2.4 GHz: 16 dBm at 1 DSSS
    - 5 GHz: 15.1 dBm at 6 OFDM
  - Wi-Fi RX sensitivity
    - 2.4 GHz: –94.5 dBm at 1 DSSS
    - 5 GHz: –89 dBm at 6 OFDM
- Additional integrated components
  - 40.0-MHz crystal
  - 32.768-kHz crystal (RTC)
  - 32Mbit SPI serial flash
  - RF filters, diplexer and passive components
- Module supports the TI SimpleLink Developer's Ecosystem

BLE/Zigbee/Thread core Features

- Microcontroller
  - 48-MHz Arm® Cortex®-M4F
  - 352KB Programmable Flash
  - 256KB of ROM for protocols and library functions
  - 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
  - 80KB of ultra-low leakage SRAM. The SRAM is protected by parity to ensure high reliability of operation.
  - 2-Pin cJTAG and JTAG debugging RF performance
  - Supports Over-the-Air upgrade (OTA)
- Ultra-low power sensor controller with 4KB of SRAM
  - Sample, store, and process sensor data
  - Operation independent from system CPU
  - Fast wake-up for low-power operation
  - BQB, FCC, CE, RoHS compliant
- TI-RTOS, drivers, Bootloader, Bluetooth® 5 Low Energy Controller, and IEEE 802.15.4 MAC in ROM for optimized application size
- Peripherals
  - Digital peripherals can be routed to any GPIO
  - 4× 32-bit or 8× 16-bit general-purpose timers
  - 12-Bit ADC, 200k Samples/s, 8 channels
  - 2× comparators with internal reference DAC
  - (1× continuous time, 1× ultra-low power)
  - Programmable current source
  - 2× UART
  - 2× SSI (SPI, MICROWIRE, TI)
  - I2C
  - I2S
  - Real-Time Clock (RTC)
  - AES 128- and 256-bit Crypto Accelerator
  - ECC and RSA Public Key Hardware Accelerator
  - SHA2 Accelerator (Full suite up to SHA-512)
  - True Random Number Generator (TRNG)
  - Capacitive sensing, up to 8 channels
  - Integrated temperature and battery monitor
- External system
  - On-chip Buck DC/DC converter
- Low power
  - Wide supply voltage range: 1.8 V to 3.8 V
  - Active-Mode RX: 6.9 mA
  - Active-Mode TX 0 dBm: 7.3 mA
  - Active-Mode TX 5 dBm: 9.6 mA
  - Active-Mode TX at +10 dBm: 22 mA
  - Active-Mode TX at +20 dBm: 85 mA
  - Active-Mode MCU 48 MHz (CoreMark):
  - 3.4 mA (71 µA/MHz)
  - Sensor Controller, Low Power-Mode, 2 MHz, running infinite loop: 30.1 µA
  - Sensor Controller, Active-Mode, 24 MHz, running infinite loop: 808 µA
  - Standby: 0.94 µA (RTC on, 80KB RAM and CPU retention)
  - Shutdown: 150 nA (wakeup on external events)
- Radio section
  - 2.4 GHz RF transceiver compatible with

Bluetooth 5 Low Energy and IEEE 802.15.4 PHY and MAC
  - Excellent receiver sensitivity:
  - 100 dBm for 802.15.4 (2.4 GHz),
  - –105 dBm for Bluetooth 125-kbps (LE Coded PHY)
  - Output power up to +20 dBm with temperature compensation
  - Suitable for systems targeting compliance with worldwide radio frequency regulations
- Wireless protocols
  - Thread, Zigbee®, Bluetooth® 5 Low Energy, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), Wi-SUN®, proprietary systems, SimpleLink™ TI 15.4-Stack (2.4 GHz), and Dynamic Multiprotocol Manager (DMM) driver.

Applications

For Internet of Things applications, such as:

- IoT Gateway
- Medical and Healthcare
  - Multiparameter Patient Monitor
  - Electrocardiogram (ECG)
  - Electronic Hospital Bed & Bed Control
  - Telehealth Systems
- Building and Home Automation:
  - HVAC Systems & Thermostat
  - Video Surveillance, Video Doorbells, and Low-Power Camera
  - Building Security Systems and E-locks
- Appliances
- Asset Tracking
- Factory Automation
- Grid Infrastructure

Contents

1. References

[1] CC3235SF Datasheet https://www.ti.com/product/CC3235SF
[2] CC3235SF User guide https://www.ti.com/lit/pdf/swru543
[3] CC2652P Datasheet https://www.ti.com/product/CC2652P
[4] CC2652P User guide https://www.ti.com/lit/pdf/swcu185

2. Block Diagram

BDE-BW20C module is based on TI CC3235SF and CC2652P with all peripherals and a dual band chip antenna, it allows faster time to market at reduced development cost.
The module, as seen in Figure 1, comprises of:

- a 32 Mbit SPI Flash
- a 48MHz XTAL
- a 40MHz XTAL
- two 32.768kHz XTALs
- two filters
- three SPDTs
- a diplexer
- a dual band chip antenna
- an U.FL connector

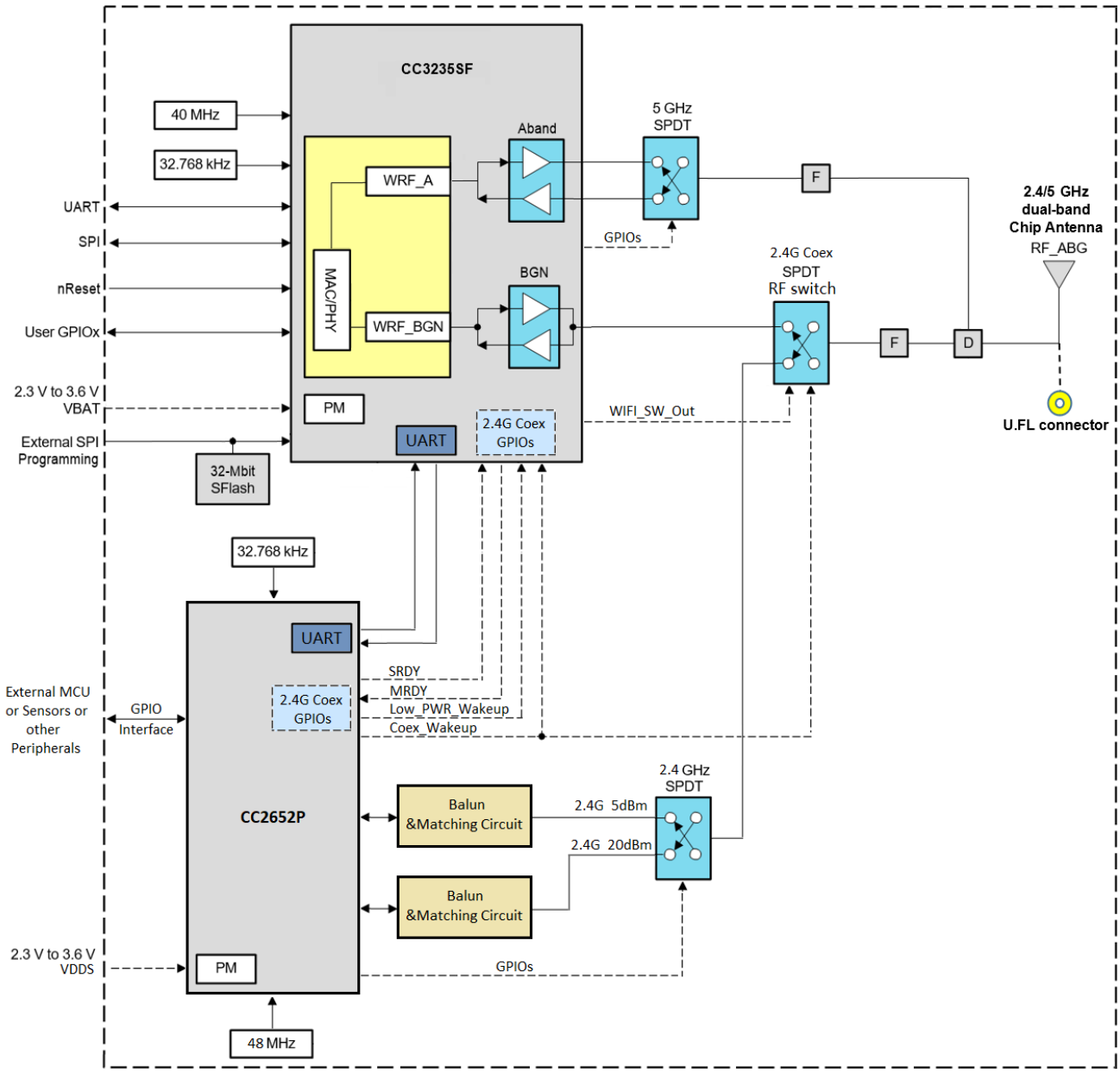

Figure 2-1. BDE-BW20C Module Block Diagram

3. Terminal Configuration and Functions

3.1 Pin Diagram

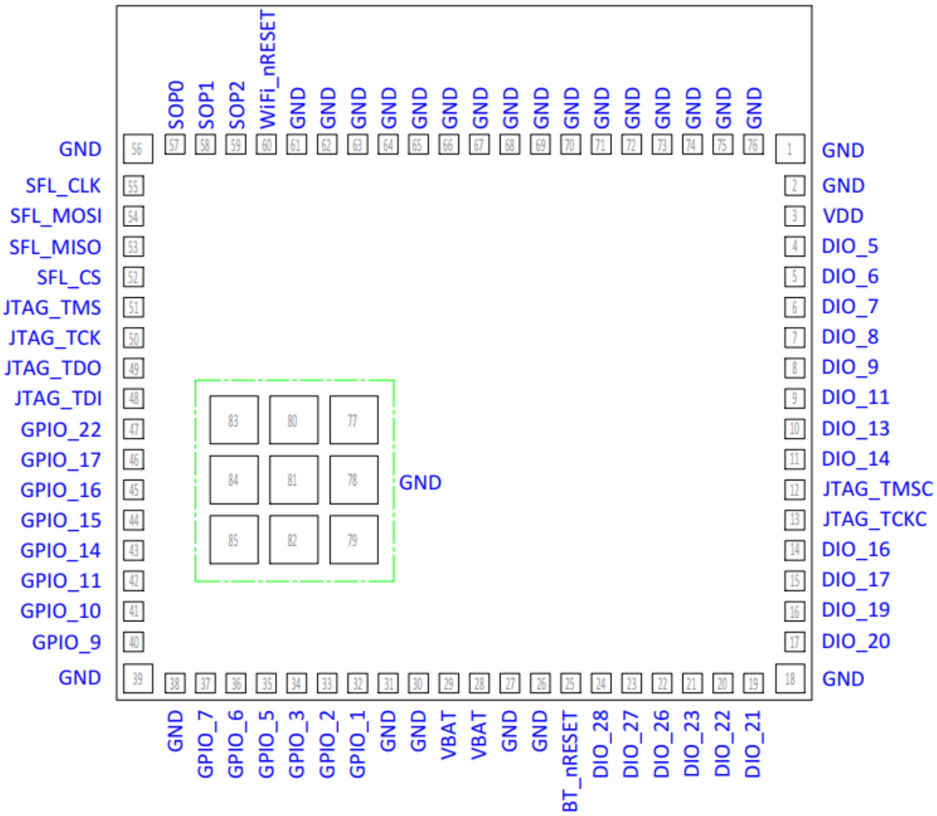

Figure 3-1. Pin Diagram Bottom View

3.2 Pin Attributes and Pin Multiplexing

Table 3-1. Pin Description

Pin #	Pin Name	Type[(1)]	Description
CC2652P:			
1	GND	–	Ground
2	GND	–	Ground
3	VDD	–	Supply power for CC2652P
4	DIO_5	I/O	GPIO, High-drive capability
5	DIO_6	I/O	GPIO, High-drive capability
6	DIO_7	I/O	GPIO, High-drive capability
7	DIO_8	I/O	GPIO
8	DIO_9	I/O	GPIO
9	DIO_11	I/O	GPIO
10	DIO_13	I/O	GPIO
11	DIO_14	I/O	GPIO
12	JTAG_TMSC	I/O	JTAG TMSC, High-drive capability
13	JTAG_TCKC	I	JTAG TCKC

Pin #	Pin Name	Type[1]	Description
14	DIO_16	I/O	GPIO, JTAG_TDO, High-drive capability
15	DIO_17	I/O	GPIO, JTAG_TDI, High-drive capability
16	DIO_19	I/O	GPIO
17	DIO_20	I/O	GPIO
18	GND	–	Ground
19	DIO_21	I/O	GPIO
20	DIO_22	I/O	GPIO
21	DIO_23	I/O	GPIO, Analog capability
22	DIO_26	I/O	GPIO, Analog capability
23	DIO_27	I/O	GPIO, Analog capability
24	DIO_28	I/O	GPIO, Analog capability
25	BT_nRESET	I	CC2652P Reset, Active low. With internal pullup resistor
26	GND	–	Ground
27	GND	–	Ground
CC3235SF:			
28	VBAT	–	Supply power for CC3235SF
29	VBAT	–	Supply power for CC3235SF
30	GND	–	Ground
31	GND	–	Ground
32	GPIO_1	I/O	GPIO
33	GPIO_2	I/O	GPIO
34	GPIO_3	I/O	GPIO
35	GPIO_5	I/O	GPIO
36	GPIO_6	I/O	GPIO
37	GPIO_7	I/O	GPIO
38	GND	–	Ground
39	GND	–	Ground
40	GPIO_9	I/O	GPIO
41	GPIO_10	I/O	GPIO
42	GPIO_11	I/O	GPIO
43	GPIO_14	I/O	GPIO
44	GPIO_15	I/O	GPIO
45	GPIO_16	I/O	GPIO
46	GPIO_17	I/O	GPIO
47	GPIO_22	I/O	GPIO
48	JTAG_TDI	I/O	JTAG TDI input. Leave unconnected if not used
49	JTAG_TDO	I/O	JTAG TDO output. Leave unconnected if not used
50	JTAG_TCK	I/O	JTAG TCK input. Leave unconnected if not used
51	JTAG_TMS	I/O	JTAG TMS input. Leave unconnected if not used
52	SFL_CS	I	External Serial Flash Programming: SPI chip select (Active low)
53	SFL_MISO	I	External Serial Flash Programming: SPI data in
54	SFL_MOSI	O	External Serial Flash Programming: SPI data out
55	SFL_CLK	I	External Serial Flash Programming: SPI clock
56	GND	–	Ground
57	SOP0	-	Used as 5 GHz switch control. An internal 100-kΩ pulldown resistor is tied to this SOP pin. An external 10-kΩ resistor is required to pull this pin high. See Section 5.8 for SOP[2:0] configuration modes.
58	SOP1	-	Used as 5 GHz switch control. An internal 100-kΩ pulldown resistor is tied to this SOP pin. An external 10-kΩ resistor is required to pull this pin high. See Section 5.8 for SOP[2:0] configuration modes.

Pin #	Pin Name	Type(1)	Description
59	SOP2	-	An internal 100-kΩ pulldown resistor is tied to this SOP pin. See Section 5.8 for SOP[2:0] configuration modes.
60	WiFi_nRESET	I	CC3235SF Reset. There is an internal 100-kΩ pullup resistor option from the nRESET pin to VBAT.
61	GND	–	Ground
62	GND	–	Ground
63	GND	–	Ground
64	GND	–	Ground
65	GND	–	Ground
66	GND	–	Ground
67	GND	–	Ground
68	GND	–	Ground
69	GND	–	Ground
70	GND	–	Ground
71	GND	–	Ground
72	GND	–	Ground
73	GND	–	Ground
74	GND	–	Ground
75	GND	–	Ground
76	GND	–	Ground
77	GND	–	Thermal ground
78	GND	–	Thermal ground
79	GND	–	Thermal ground
80	GND	–	Thermal ground
81	GND	–	Thermal ground
82	GND	–	Thermal ground
83	GND	–	Thermal ground
84	GND	–	Thermal ground
85	GND	–	Thermal ground

(1) I = input; O = output; I/O = bidirectional

3.3 Pad State After Application of Power to Chip, but Before Reset Release

When a stable power is applied to the BDE-BW20C module for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5V, the level of the digital pads are undefined in the period starting from the release of nRESET pins(WiFi_nRESET and BT_nRESET), until the DIG_DCDC of the CC3235SF and the DCDC_SW of the CC2652P chip power up. This period is less than approximately 10ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of these external pullup or pulldown resistors is 2.7kΩ.

3.4 Connections for Unused Pins

All unused pin should be configured as stated in Table 3-2.

Table 3-2. Connections for Unused Pins

FUNCTION	SIGNAL DESCRIPTION	PIN NUMBER	ACCEPTABLE PRACTICE
GPIO	General-purpose input or output		Wake up I/O source should not be floating during hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused GPIOs as NC
SOP	Configuration sense-on-power	57, 58, 59	Leave as NC (Modules contain internal 100-kΩ pulldown resistors on the SOP lines). An external 10-kΩ pullup resistor is required to pull these pins high. See Section 5.8 for SOP[2:0] configuration modes.
nReset	RESET input for the device	25, 60	Never leave the reset pin floating
JTAG	JTAG interface		Leave as NC if unused

4. Specifications

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)[1] [2]

4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
V_{BAT}	–0.5	3.8	V
Digital I/O	–0.5	V_{BAT} + 0.5	V
Analog pins	–0.5	2.1	V
Operating temperature (T_A)	–40	85	°C
Storage temperature (T_{stg})	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)		±2000	V
	Charged device model (CDM), per JESD22-C101(2)	All pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (2) (1) (3)

PARAMETER	MIN	TYP	MAX	UNIT
V_{BAT}	2.3	3.3	3.6	V
Operating temperature	–40	25	85	°C
Ambient thermal slew	–20		20	°C/minute

(1) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(2) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV. The ripple should not cause the supply to fall below the brownout voltage.
(3) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

4.4 Brownout and Blackout Conditions

The module enters a brownout condition whenever the input voltage dips below $V_{BROWNOUT}$ (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (four contacts for a 2× AA battery), and the wiring and PCB routing resistance.

Note

When the module is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

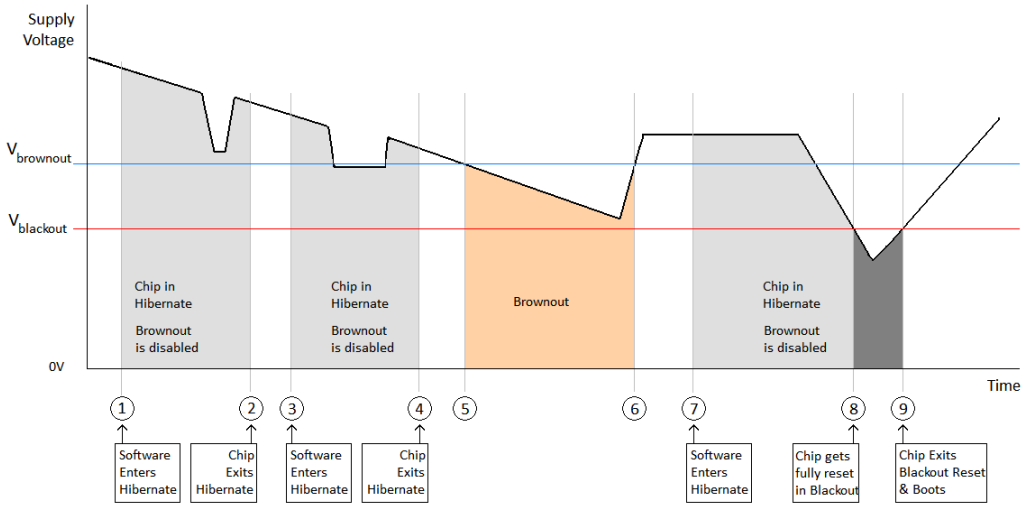

Figure 4-1. Brownout and Blackout Levels (1 of 2)

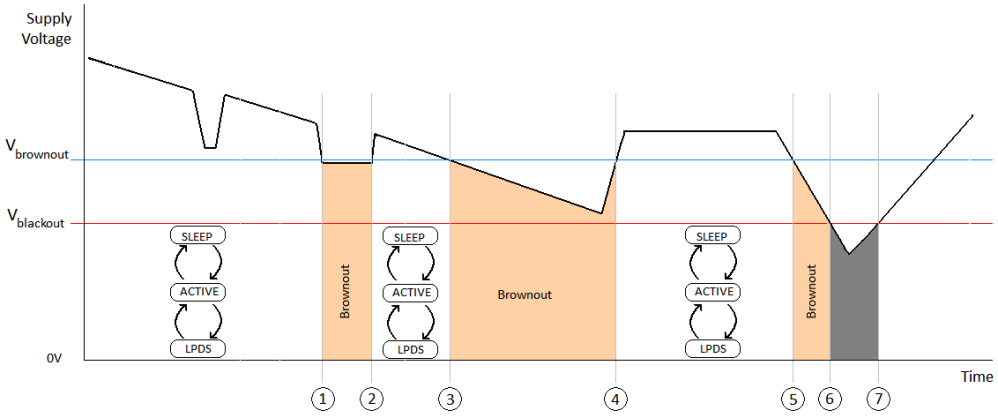

Figure 4-2. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA.

The blackout condition is equivalent to a hardware reset event in which all states within the module are lost. $V_{brownout}$ = 2.1 V and $V_{blackout}$ = 1.67 V

Table 4-2 lists the brownout and blackout voltage levels.

Table 4-2. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

4.5 Electrical Characteristics for GPIO Pins

Table 4-3. GPIO Pins (25°C) (1)

T_A = 25°C, V_{BAT} = 3.3 V

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA;			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA;			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA;			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA;			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA;		V_{DD} × 0.2		V
			IL = 4 mA; configured I/O drive strength = 4 mA;		V_{DD} × 0.2		
			IL = 6 mA; configured I/O drive strength = 6 mA;		V_{DD} × 0.2		
			IL = 2 mA; configured I/O drive strength = 2 mA;		V_{DD} × 0.25		
I_{OH}	High-level source current	2-mA drive			2		mA
		4-mA drive			4		
		6-mA drive			6		
I_{OL}	Low-level sink current	2-mA drive			2		mA
		4-mA drive			4		
		6-mA drive			6		

(1) We recommend using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

Table 4-4. Electrical Characteristics for Pin Internal Pullup and Pulldown (25°C)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{OH}	Pullup current (V_{DD} = 3.0 V)			10		µA
I_{OL}	Pulldown current (V_{DD} = 3.0 V)			10		µA

4.6 Reset Requirement

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	Operation mode level		0.65 × V_{BAT}		V
V_{IL}	Shutdown mode level(1)	0	0.6		V
	Minimum time for nReset low for resetting the module	5			ms
T_r and T_f	Rise and fall times		20		µs

(1) The nRESET pins must be held below 0.6 V for the module to register a reset.

4.7 Timing and Switching Characteristics

4.7.1 Power-Up Sequencing

For proper start-up of the BDE-BW20C module, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT1} (pin 37) and V_{BAT2} (pin 40) together on the board.
2. Hold the nRESET pins low while the supplies are ramping up.

Figure 4-3 shows the reset timing diagram for the first-time power-up and reset removal.

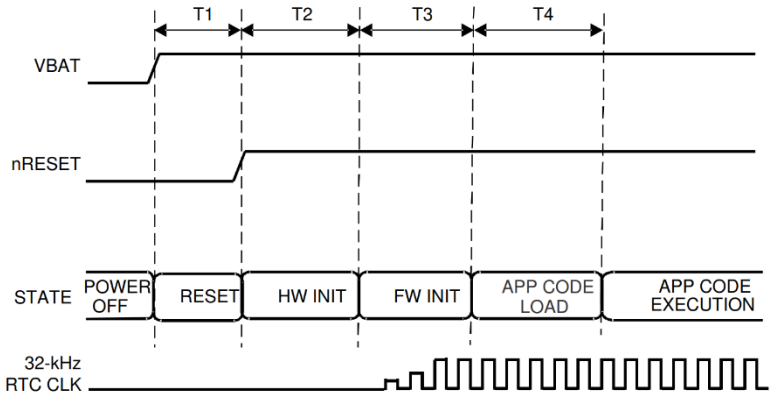

Figure 4-3. First-Time Power-Up and Reset Removal Timing Diagram

4.7.2 Power-Down Sequencing

For proper power down of the BDE-BW20C module, ensure that the nRESET (pin 25, pin60) and nHIB (pin 4) pins have remained in a known state for a minimum of 200 ms before removing power from the module.

4.7.3 Device Reset

When a device restart is required, issue a negative pulse to the nRESET pins. Ensure the reset is properly applied: A negative reset pulse (on pin 35) of at least 200-mS duration.

4.7.4 Wake Up From Hibernate Timing

Table 4-5 lists the software hibernate timing requirements.

Note

The internal 32.768-kHz crystal is kept enabled by default when the module goes to hibernate.

Table 4-5. Software Hibernate Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{HIB_MIN}	Minimum hibernate time		10			ms
$T_{wake\_from\_hib}$(1)	Hardware wakeup time plus firmware initialization time			50(2)		ms
T_APP_CODE_LOAD	App code load time for BDE-BW20C	BDE-BW20C		Image size (KB) × 0.06		ms

(1) $T_{wake\_from\_hib}$ can be 200ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.

(2) Wake-up time can extend to 75ms if a patch is downloaded from the serial flash.

Figure 4-4 shows the timing diagram for wake up from the hibernate state.

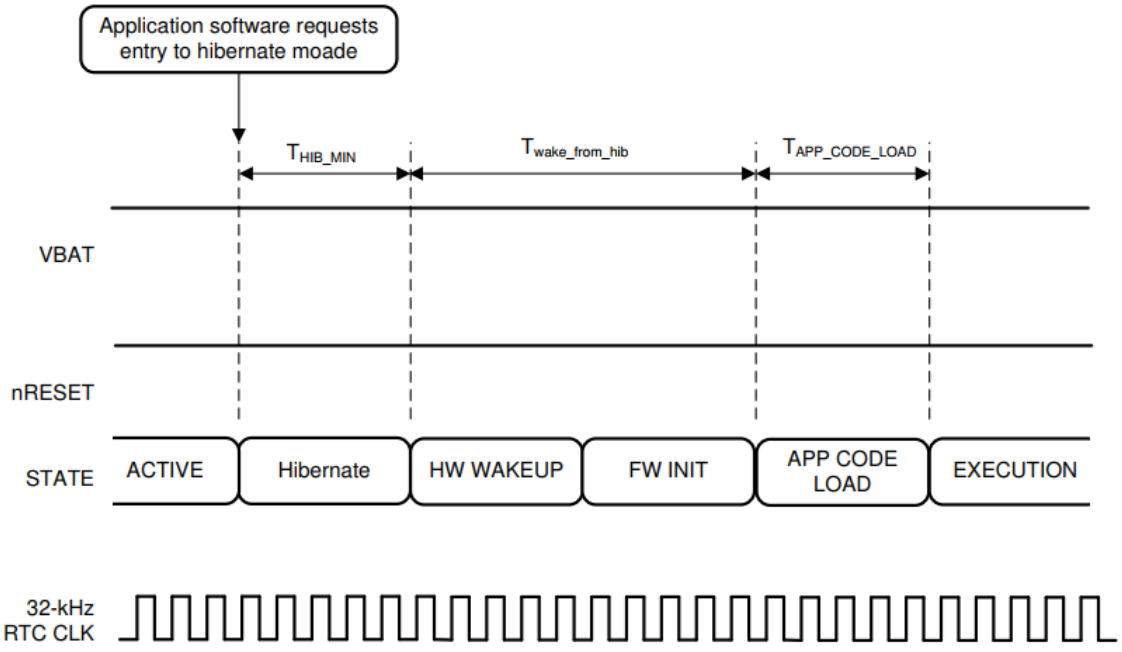

Figure 4-4. Wake Up From Hibernate Timing Diagram

4.7.5 Peripherals Timing

This section describes the peripherals that are supported by the BDE-BW20C module, as follows:

- SPI
- I²S
- GPIOs
- I²C
- IEEE 1149.1 JTAG
- ADC
- Camera parallel port
- External flash
- UART
- SD Host
- Timers

4.7.5.1 SPI

➢ **SPI Master**

The BDE-BW20C module includes three SPIs, one in CC3235SF and two in CC2652P, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 4-5 shows the timing diagram for the SPI master.

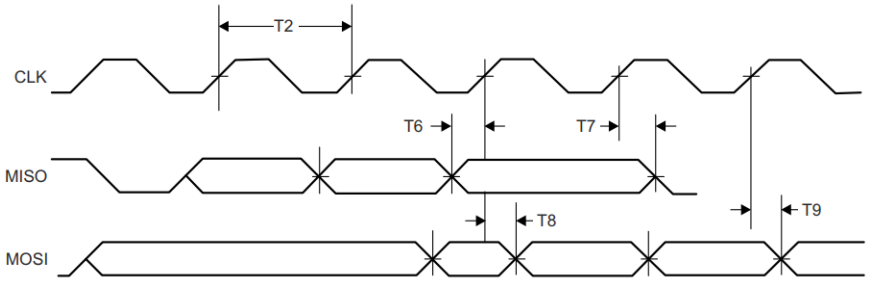

Figure 4-5. SPI Master Timing Diagram

Table 4-6 lists the timing parameters for the SPI master.

Table 4-6. SPI Master Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	$F^{(1)}$	Clock frequency		20	MHz
T2	$T_{clk}^{(1)}$	Clock period	50		ns
	$D^{(1)}$	Duty cycle	45%	55%	
T6	$t_{IS}^{(1)}$	RX data setup time	1		ns
T7	$t_{IH}^{(1)}$	RX data hold time	2		ns
T8	$t_{OD}^{(1)}$	TX data output delay		8.5	ns
T9	$t_{OH}^{(1)}$	TX data hold time		8	ns

(1) Timing parameter assumes a maximum load of 20 pF.

➢ **SPI Slave**

Figure 4-6 shows the timing diagram for the SPI slave.

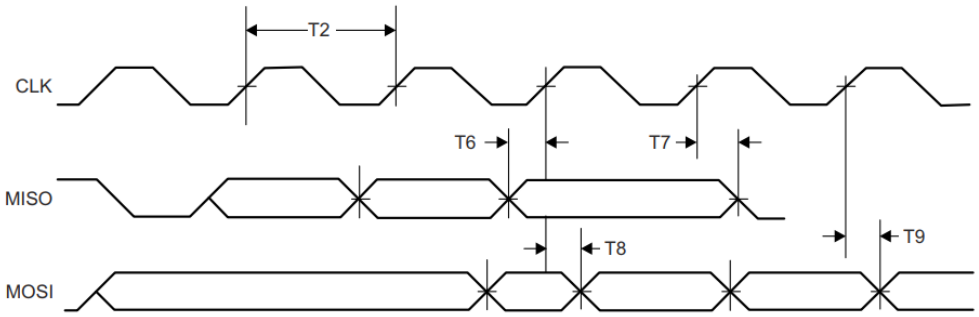

Figure 4-6. SPI Slave Timing Diagram

Table 4-7 lists the timing parameters for the SPI slave.

Table 4-7. SPI Slave Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	$F^{(1)}$	Clock frequency @ VBAT = 3.3 V		20	MHz
		Clock frequency @ VBAT ≤ 2.3 V		12	
T2	$T_{clk}^{(1)}$	Clock period	50		ns
	$D^{(1)}$	Duty cycle	45%	55%	
T6	$t_{IS}^{(1)}$	RX data setup time	4		ns
T7	$t_{IH}^{(1)}$	RX data hold time	4		ns
T8	$t_{OD}^{(1)}$	TX data output delay		20	ns
T9	$t_{OH}^{(1)}$	TX data hold time		24	ns

(1) Timing parameter assumes a maximum load of 20pF at 3.3V.

4.7.5.2 I2S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

- **I2S Transmit Mode**

Figure 4-7 shows the timing diagram for the I2S transmit mode.

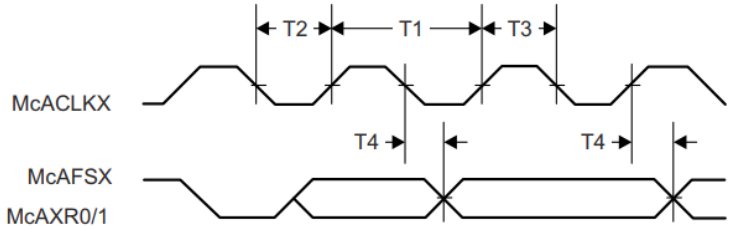

Figure 4-7. I2S Transmit Mode Timing Diagram

Table 4-8 lists the timing parameters for the I2S transmit mode.

Table 4-8. I2S Transmit Mode Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t_{LP} (1)	Clock low period		1/2 fclk	ns
T3	t_{HT} (1)	Clock high period		1/2 fclk	ns
T4	t_{OH} (1)	TX data hold time		22	ns

(1) Timing parameter assumes a maximum load of 20 pF.

- **I2S Receive Mode**

Figure 4-8 shows the timing diagram for the I2S receive mode.

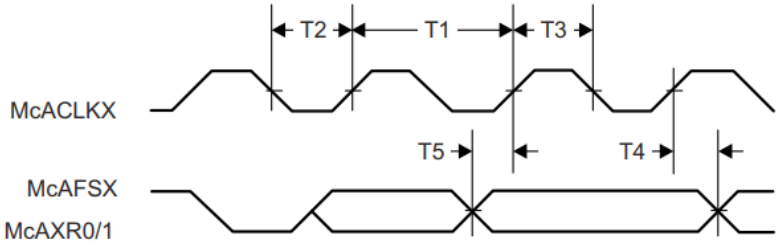

Figure 4-8. I2S Receive Mode Timing Diagram

Table 4-9 lists the timing parameters for the I2S receive mode.

Table 4-9. I2S Receive Mode Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t_{LP} (1)	Clock low period		1/2 f_{clk}	ns
T3	t_{HT} (1)	Clock high period		1/2 f_{clk}	ns
T4	t_{OH} (1)	RX data hold time		0	ns
T5	t_{OS} (1)	RX data setup time		15	ns

(1) Timing parameter assumes a maximum load of 20 pF.

4.7.5.3 GPIOs

All digital pins of the module can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 4-9 shows the GPIO timing diagram.

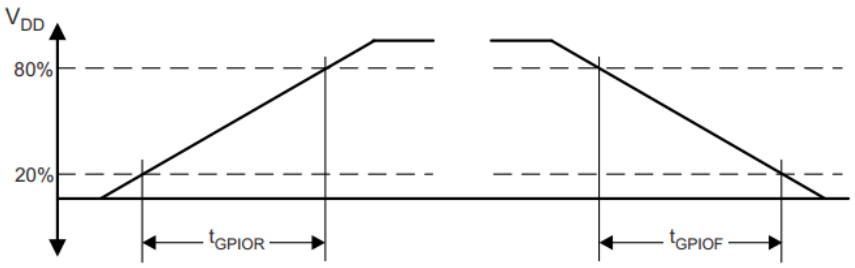

Figure 4-9. GPIO Timing Diagram

Table 4-10 lists the GPIO output transition times for V_{BAT} = 2.3 V.

Table 4-10. GPIO Output Transition Times (VBAT = 2.3 V)(1) (2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r			T_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1 4MA_EN=0	11.7	13.9	16.3	11.5	13.9	16.7	ns
4	2MA_EN=0 4MA_EN=1	13.7	15.6	18.0	9.9	11.6	13.6	ns
6	2MA_EN=1 4MA_EN=1	5.5	6.4	7.4	3.8	4.7	5.8	ns

(1) V_{BAT} = 2.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 25, 26, 42, and 44.

Table 4-11 lists the GPIO output transition times for V_{BAT} = 3.3 V.

Table 4-11. GPIO Output Transition Times (VBAT = 3.3 V)(1) (2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r			T_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1 4MA_EN=0	8.0	9.3	10.7	8.2	9.5	11.0	ns
4	2MA_EN=0 4MA_EN=1	6.6	7.1	7.6	4.7	5.2	5.8	ns
6	2MA_EN=1 4MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9	ns

(1) V_{BAT} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52 and 53.

Table 4-12 lists the input transition time parameters.

Table 4-12. GPIO Input Transition Time Parameters

		MIN	MAX	UNIT
t_r	Input transition time (t_r, t_f), 10% to 90%	1	3	ns
t_f		1	3	ns

4.7.5.4 I²C

The BDE-BW20C module includes two I²Cs in CC3235SF and CC2652P respectively operating with standard (100 kbps) or fast (400 kbps) transmission speeds.
Figure 4-10 shows the I²C timing diagram.

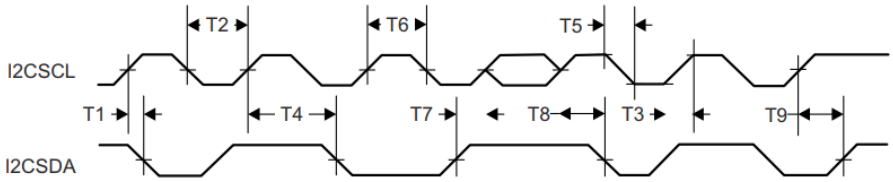

Figure 4-10. I²C Timing Diagram

Table 4-13 lists the I²C timing parameters.

Table 4-13. I²C Timing Parameters(3)

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T2	t_{LP}	Clock low period	See (1)		System clock
T3	t_{SRT}	SCL/SDA rise time		See (2)	ns
T4	t_{DH}	Data hold time	NA		
T5	t_{SFT}	SCL/SDA fall time	3		ns
T6	t_{HT}	Clock high time	See (1)		System clock
T7	t_{DS}	Data setup time	tLP/2		System clock
T8	t_{SCSR}	Start condition setup time	36		System clock
T9	t_{SCS}	Stop condition setup time	24		System clock

(1) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(2) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the value of the external signal capacitance and external pullup register.
(3) All timing is with 6-mA drive and 20-pF load.

4.7.5.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary-Scan Architecture*.

Figure 4-11 shows the JTAG timing diagram.

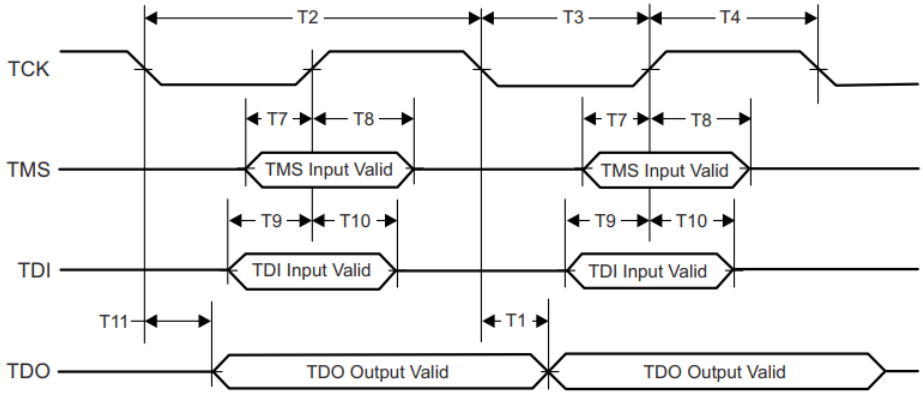

Figure 4-11. JTAG Timing Diagram

Table 4-14 lists the JTAG timing parameters.

Table 4-14. JTAG Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{TCK}	Clock frequency		15	MHz
T2	t_{TCK}	Clock period		1 / f_{TCK}	ns
T3	t_{CL}	Clock low period		t_{TCK} / 2	ns
T4	t_{CH}	Clock high period		t_{TCK} / 2	ns
T7	t_{TMS_SU}	TMS setup time	1		ns
T8	t_{TMS_HO}	TMS hold time	16		ns
T9	t_{TDI_SU}	TDI setup time	1		ns
T10	t_{TDI_HO}	TDI hold time	16		ns
T11	t_{TDO_HO}	TDO hold time		15	ns

4.7.5.6 ADC

Table 4-15 lists the ADC electrical specifications. See *CC32xx ADC Appnote* for further information on using the ADC and for application-specific examples.

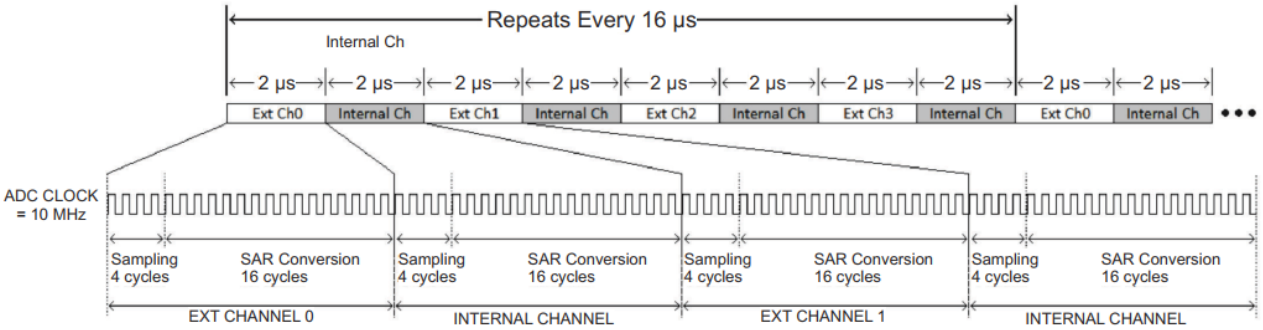

Figure 4-12. ADC Clock Timing Diagram

Figure 4-12 shows the ADC clock timing diagram.

Table 4-15. ADC Electrical Specifications

PARAMETER	DESCRIPTION	TEST CONDITIONS / ASSUMPTIONS	MIN	TYP	MAX	UNIT
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–2.5		2.5	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–1		4	LSB
Input range			0		1.4	V
Driving source impedance					100	Ω
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				12		pF
Input impedance		ADC Pin 57		2.15		kΩ
		ADC Pin 58		0.7		
		ADC Pin 59		2.12		
		ADC Pin 60		1.17		
Number of channels				4		
F_{sample}	Sampling rate of each pin			62.5		KSPS
F_input_max	Maximum input signal frequency				31	kHz
SINAD	Signal-to-noise and distortion	Input frequency DC to 300 Hz and 1.4 V_{pp} sine wave input	55	60		dB
I_active	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
I_PD	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
Absolute offset error		FCLK = 10 MHz		±2		mV
Gain error				±2%		
V_{ref}	ADC reference voltage			1.467		V

4.7.5.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 4-13 shows the timing diagram for the camera parallel port.

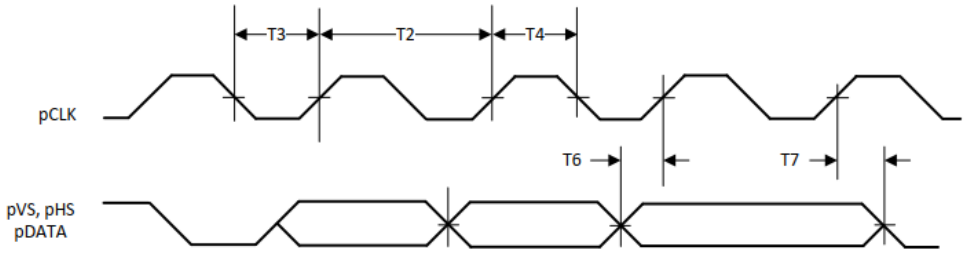

Figure 4-13. Camera Parallel Port Timing Diagram

Table 4-16 lists the timing parameters for the camera parallel port.

Table 4-16. Camera Parallel Port Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	pCLK	Clock frequency		2	MHz
T2	T_{clk}	Clock period		1/pCLK	ns
T3	t_{LP}	Clock low period		T_{clk}/2	ns
T4	t_{HT}	Clock high period		T_{clk}/2	ns
T6	t_{IS}	RX data setup time		2	ns
T7	t_{IH}	RX data hold time		2	ns

4.7.5.8 UART

Except two UARTs connected between CC2652P and CC3235SF, the BDE-BW20C module includes other two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using µDMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

4.7.5.9 External Flash Interface

The BDE-BW20C module includes the Macronix™ 32-Mbit serial flash. The serial flash can be programmed directly using the external flash interface (pins 13, 14, 15, and 17). During normal operation, the external flash interface should remain unconnected.

For timing details, see the MX25R3235F data sheet.

4.7.5.10 SD Host

The BDE-BW20C module provides an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3235x platform, we recommend that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3235x Software Development Kit (SDK).

The SD host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2 GB) cards HC SD
- Flexible architecture, allowing support for new command structure.
- 1-bit transfer mode specifications for SD cards
- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24 MHz

4.7.5.11 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The general-purpose timer module (GPTM) of the BDE-BW20C module contains 16- or 32-bit GPTM blocks. In CC3235SF, each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger µDMA transfers. While CC2652P contains 4× 32-bit or 8× 16-bit general-purpose timers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller (µDMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80 MHz)

5. Detailed Description

5.1 Overview

BDE-BW20C is a dual processor low power IoT network gateway module integrates multiple wireless technologies and protocols which include 2.4GHz and 5GHz Dual-Band Wi-Fi 802.11a/b/g/n, Bluetooth 5.1 Low Energy, BLE mesh, Thread, Zigbee, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), Wi-SUN, proprietary systems, SimpleLink TI 15.4-Stack (2.4 GHz) and Dynamic Multiprotocol Manager (DMM) driver.
The module combines a low power Dual-Band Wi-Fi SoC CC3235SF and a 2.4GHz low power multiprotocol wireless SoC CC2652P with all external components including a Dual-band chip antenna. Both SoCs are integrated with an Arm® Cortex®-M4 application MCU and are able to run independently with Wi-Fi/BLE Coexistence design.

5.2 Arm Cortex-M4 Processor Core Subsystem

The CC3235SF contains a high-performance Arm Cortex-M4 processor which provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even

while SYSRESETn is asserted

– Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
– Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

The CC2652P SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.
The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.
Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  – Data Watchpoint and Trace Unit (DWT)
  – JTAG Debug Access Port (DAP)
  – Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  – Instrumentation Trace Macrocell Unit (ITM)
  – Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

5.3 Security

The BDE-BW20C internet-on-a chip module enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2

- Secure sockets
  - Protocol versions: SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256

  - Server authentication
  - Client authentication
  - Domain name verification
  - Runtime socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog – Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key – Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery – Allows encrypted file transfer to the system using asymmetric keys created by the device

Code and Data Security:

- Network passwords and certificates are encrypted and signed
- Cloning protection – Application and data files are encrypted by a unique key per device
- Access control – Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lockdown mechanism takes effect
- Encrypted and authenticated file system
- Secured boot – Authentication of the application image on every boot
- Code and data encryption – User application and data files are encrypted in sFlash
- Code and data authentication – User Application and data files are authenticated with a public key certificate
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer
- Recovery mechanism

Device Security:

- Separate execution environments – Application processor and network processor run on separate Arm cores
- Initial secure programming – Allows for keeping the content confidential on the production line
- Debug security
  - JTAG lock
  - Debug ports lock
- True random number generator

5.4 Power-Management Subsystem

The BDE-BW20C power-management subsystem contains DC/DC converters to accommodate the differing voltage or current requirements of the system.

The BDE-BW20C module is a fully integrated module-based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

In the wide-voltage battery connection, the module can be directly connected to two AA alkaline batteries. All other voltages required to operate the module are generated internally by the DC/DC converters. This scheme is the most common mode for the module because it supports wide-voltage operation from 2.3 to 3.6 V.

5.5 Low-Power Operating Mode

From a power-management perspective, the BDE-BW20C module comprises the following two independent subsystems:

- Arm Cortex-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm Cortex-M4 application processor runs the user application loaded from an internal serial flash, or on-module XIP flash. The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 5-1.

Table 5-1. User Program Modes

APPLICATION PROCESSOR (MCU) MODE(1)	DESCRIPTION
MCU active mode	MCU executing code at 80-MHz state rate.
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO.
MCU shutdown mode	The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1 s. To enter or exit the shutdown mode, the state of the nRESET lines are changed (low to shut down, high to turn on).

(1) Modes are listed in order of power consumption, with highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 5-2).

Table 5-2. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode (processing layer 3, 2, and 1)	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The BDE-BW20C NWPs automatically go into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake up.
Network disabled	The network is disabled

The operation of the application and network processor ensures that the module remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

5.6 Internal Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data in CC2652P. The flash memory is insystem programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU.
The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area(CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets. The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

The CC3235SF device within the BDE-BW20C module includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3235SF device ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3235SF API list.

5.6.1 SRAM

The BDE-BW20C module provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

5.6.2 ROM

The internal zero-wait-state ROM of the BDE-BW20C module is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The DriverLib software library of the BDE-BW20C module controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt- driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory to be used for other purposes.

5.6.3 Flash Memory

The CC3235SF device within the BDE-BW20C modules comes with an on-chip flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The flash memory is used for code and constant data sections and is directly attached to the ICODE/ DCODE bus of the Arm Cortex-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The flash memory is organized as 2-KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

5.6.4 Memory Map

Table 5-3 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 5-3. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (bootloader + DriverLib)	
0x0100 0000	0x010F FFFF	On-chip flash (for user application code)	
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 to 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x4000 07FF	I^2C A0 (master)	
0x4002 4000	0x4002 4FFF	GPIO group 4	
0x4002 0800	0x4002 0FFF	I^2C A0 (slave)	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000 0000 to 0x400F FFFF	
0x4401 0000	0x4401 0FFF	SDIO master	
0x4401 8000	0x4401 8FFF	Camera Interface	
0x4401 C000	0x4401 DFFF	McASP	
0x4402 0000	0x4402 0FFF	SSPI	Used for external serial flash
0x4402 1000	0x4402 1FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum	
0x4403 5000	0x4403 5FFF	MD5/SHA	
0x4403 7000	0x4403 7FFF	AES	
0x4403 9000	0x4403 9FFF	DES	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	NVIC	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

5.7 Restoring Factory Default Configuration

The CC3235SF in BDE-BW20C module has an internal recovery mechanism that rolls back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling software APIs, or by pulling or forcing SOP[2:0] = 011 pins and toggling the WiFi_nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial flash vendor.

5.8 Boot Modes

The BDE-BW20C module implements a sense-on-power (SoP) scheme to determine the device operation mode.

SoP values are sensed from the module pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0). Table 5-4 lists the pull configurations.

BDE-BW20C contains internal pulldown resistors on the SOP[2:0] lines. The application can use SOP2 for other functions after chip has powered up. However, to avoid spurious SOP values from being sensed at power up, we strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are used as 5 GHz control switch and are not available for other functions.

Table 5-4. BDE-BW20C Functional Configurations

NAME	SOP[2]	SOP[1]	SOP[0]	SoP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory, lab flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection. The default configuration for BDE-BW20C module.

NAME	SOP[2]	SOP[1]	SOP[0]	SoP MODE	COMMENT
UARTLOAD_FUNCTIONAL_4WJ	Pulldown	Pullup	Pulldown	LDfrUART_FnWJ	Supports flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the
RET_FACTORY_IMAGE	Pulldown	Pullup	Pullup	RetFactDef	When module WiFi_nRESET is toggled, the MCU bootloader kickstarts the procedure to restore factory default images.

5.9 Hostless Mode

The BDE-BW20C device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet
- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

Note

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
- The scripter is limited to 16 pairs of conditions and reactions.
- Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
- Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.

5.10 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

A Packet Traffic Arbitrator (PTA) scheme is available for the managed coexistence of BLE and a co-located 2.4-GHz radio. This is based on 802.15.2 recommendations and common industry standards. The 3-wire coexistence interface has multiple modes of operation, encompassing different use cases and number of lines used for signaling. The radio acting as a slave is able to request access to the 2.4-GHz ISM band, and the master to grant it. Information about the request priority and TX or RX operation can also be conveyed.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

5.10.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API. The Bluetooth 5.2 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time. Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

5.10.2 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2

Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

6. Applications, Implementation, and Layout

6.1 Typical Application Schematic

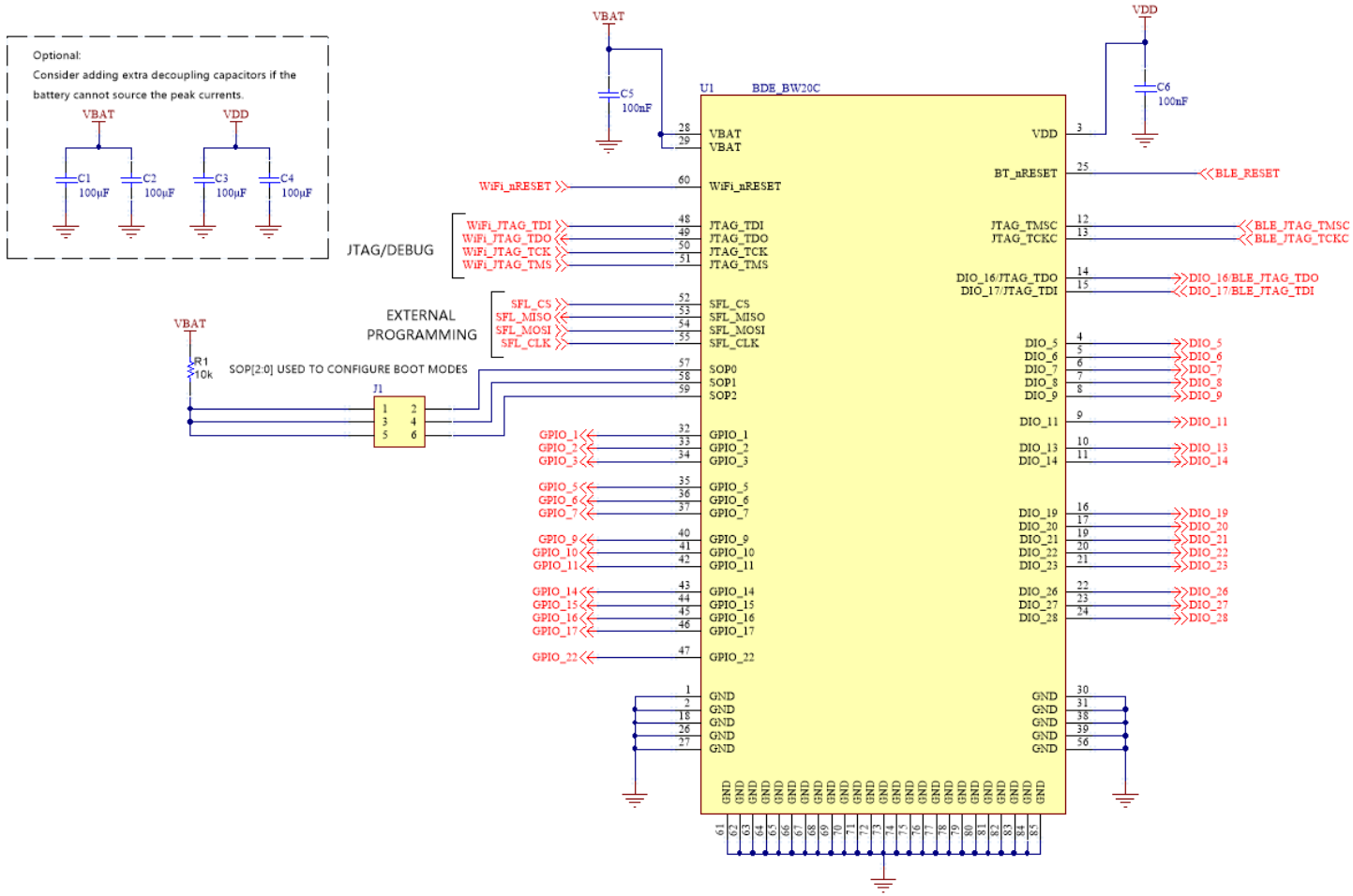

Figure 6-1. BDE-BW20C Typical Application Schematic

Table 6-1 provides the bill of materials for a typical application using the BDE-BW20C module in Figure 6-1.

Table 6-1. Bill of Materials

QTY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
4	C1, C2, C3, C4	100 µF	Murata	GRM21BR60J107ME15#	Capacitor, ceramic, 100 µF, 10 V, ±10%, X5R, 0805
2	C5, C6	100 nF	Murata	GRM033R61A104KE84#	Capacitor, ceramic, 100 nF, 10 V, ±20%, X5R, 0201
1	R1	10 k	RALEC	RTT01103JTH	RES, 10k, 5%, 0.063 W, AEC-Q200 Grade 0, 0201
1	J1	2 x 3P	Ckmtw	210-1S-2*3P	DIP, 180°, 1.27mm, 1mm, PA6T
1	U1	BDE-BW20C	BDE	BDE-BW20C	Wi-Fi/BLE/Zigbee/Thread Combo Module

6.2 Device Connection and Layout Fundamentals

6.2.1 Power Supply Decoupling and Bulk Capacitors

Depending upon routing resistors and battery type, we recommend adding two 100-µF ceramic capacitors to help provide the peak current drawn by the BDE-BW20C module.

6.2.2 Reset

The module features an internal RC circuit to reset the device during power ON. The nRESET pins must be held below 0.6 V for at least 5 ms for the device to successfully reset.

6.2.3 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current.

6.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the BDE-BW20C. We recommend customers follow the guidelines described in this section to achieve similar performance to that obtained with our reference design.

Ensure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.

Use the following guidelines to lay out the BDE-BW20C module with a chip antenna, as shown in Figure 6-2.

- The module must have a 5.3 mm clearance on all layers (no copper) to the left and right of the module placement.
- There must be at least one ground-reference plane under the module on the main PCB.

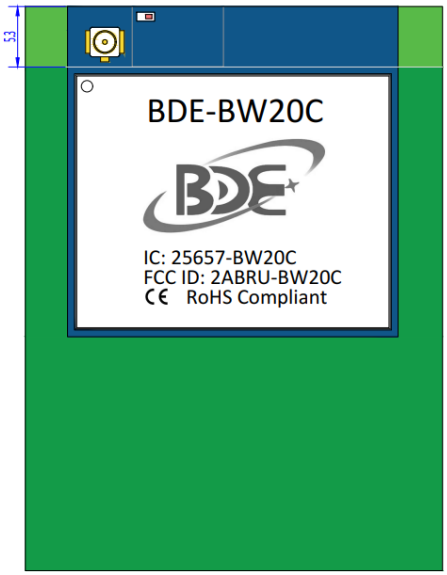

Figure 6-2. BDE-BW20C Layout Guidelines

7. Mechanical Specifications

7.1 Dimensions

The module dimensions are presented in the following figure:
Note: All dimensions are in mm.

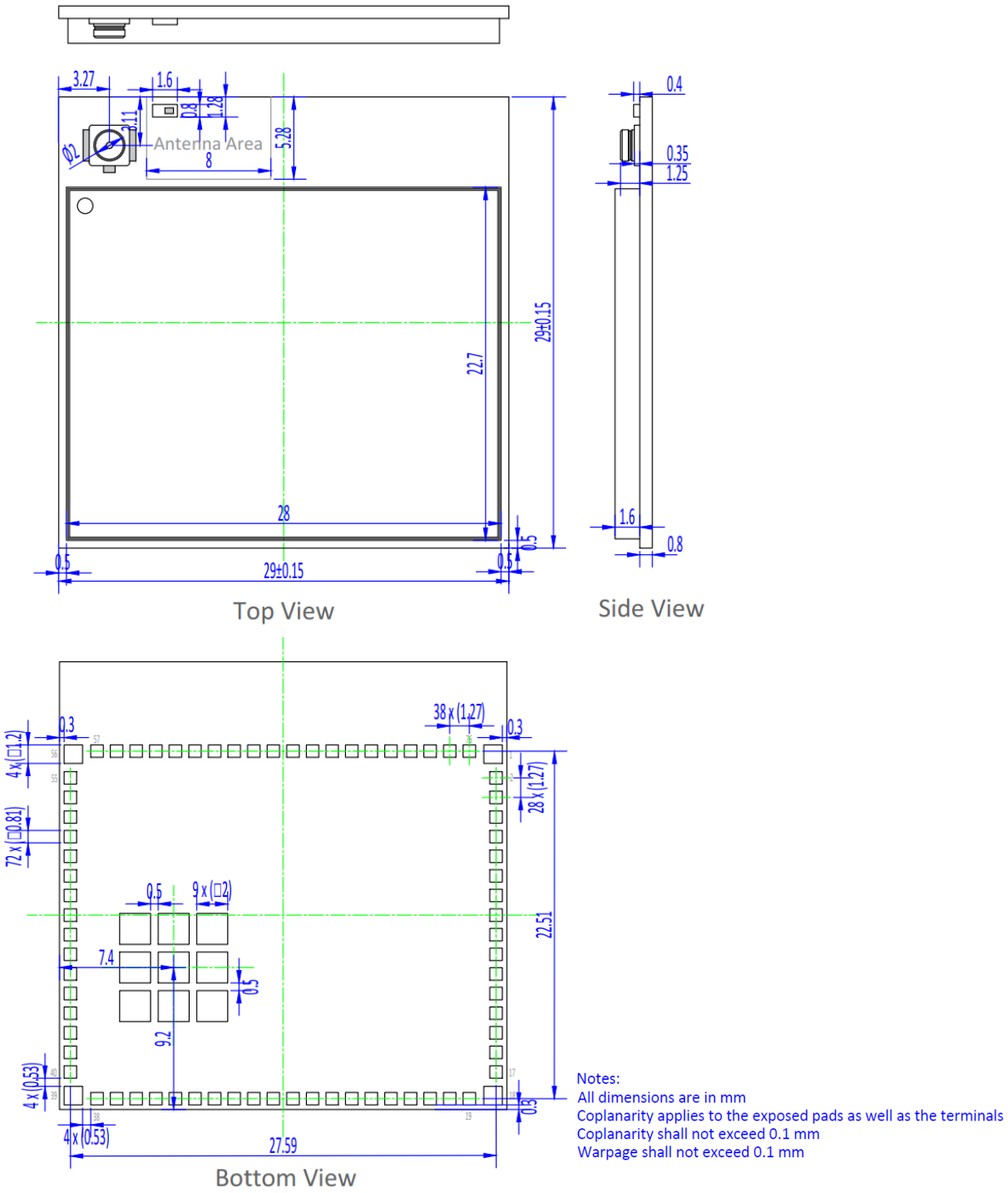

Figure 7-1. Mechanical Drawing

7.2 PCB Footprint

The footprint for the PCB is presented in the following figure:
Note: All dimensions are in mm.

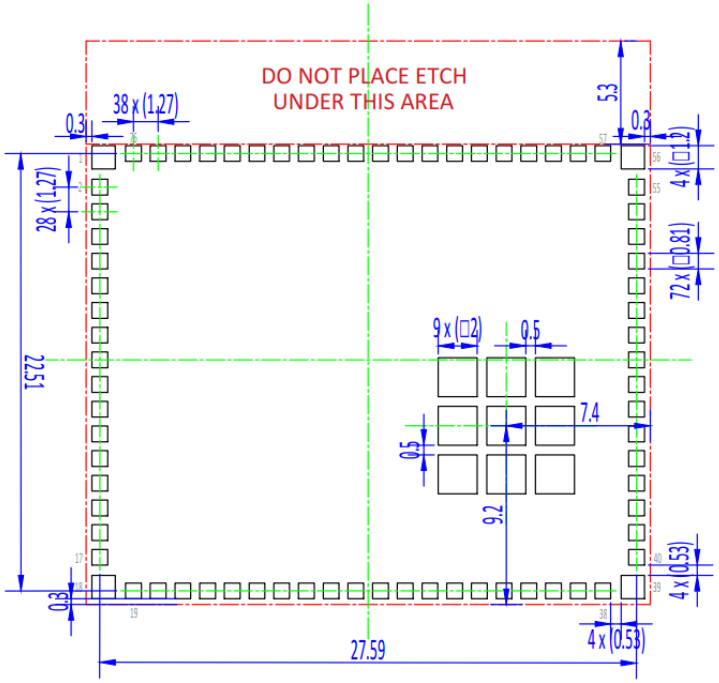

Figure 7-2. Module Footprint Top View

7.3 Marking

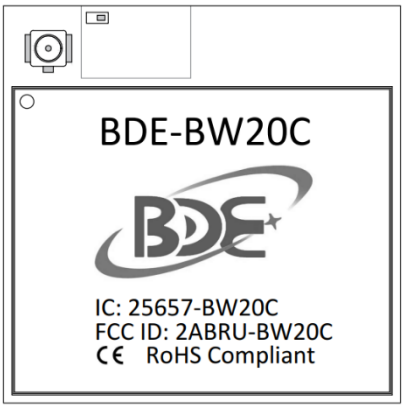

Figure 7-3. Indicative Module Shield Marking

8. Ordering Information

Part Number	Size (mm)	Flash	Core Chip	Shipping Form	MOQ
BDE-BW20CS	29 x 29 x 2.4	4MB sFlash	CC2652P + CC3235S	Tape & Reel	1000
BDE-BW20CSF	29 x 29 x 2.4	1MB + 4MB sFlash	CC2652P + CC3235SF	Tape & Reel	1000

9. Revision History

Revision	Date	Description
V1.0	8-Jan-2021	Initial Release
V1.1	14-Apr-2021	Editorial Correction

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