General Description

BDE-BW3351xPx is a 2.4-GHz and 5-GHz Dual-Band Wi-Fi 6 and Bluetooth Low Energy Combo wireless module based on TI's 10th generation connectivity combo chip CC3351 which is based upon proven technology and complements the TI integrated devices for connectivity portfolio. This module is ideal for use in cost sensitive embedded applications with a Linux or RTOS host running TCP/IP, where the peak throughput requirement is 50 Mbps maximum at the IP layer. BDE-BW3351xPx could be the best choice for bringing the efficiency of Wi-Fi 6 to embedded device applications with a small PCB footprint and highly optimized bill of materials with lower cost.

In order to fulfil different integration requirements, BDE provides different options including:

- BDE-BW3351NP1, single antenna port without antenna;
- BDE-BW3351UP1, single antenna port with U.FL connector;
- BDE-BW3351AP1, single antenna with integrated PCB antenna;
- BDE-BW3351NP2, dual antenna ports with antenna diversity without antenna;
- BDE-BW3351UP2, dual antenna ports with antenna diversity with integrated U.FL connector;
- BDE-BW3351AP2, dual antenna with antenna diversity with integrated PCB antenna (TBD).

Key Features

- Highly optimized 2.4-GHz and 5-GHz Dual-Band Wi-Fi 6 and Bluetooth Low Energy 5.2 system for low cost embedded IoT applications
- Seamless integration with TI Sitara MPU (Linux) / MCU+ (FreeRTOS) as well as other application processors
- 3-wire or 1-wire PTA for external coexistence with additional 2.4GHz radios (e.g. Thread or Zigbee)
- Multirole support e.g. STA and AP to connect directly with other Wi-Fi devices on different RF channels (Wi-Fi networks)
- Optional antenna diversity or selection (BDE-BW3351NP2, BDE-BW3351UP2)
- Operating temperature: -40°C to +85°C
- 2.4-GHz and 5-GHz Dual-Band Wi-Fi 6®
  - MAC, Baseband and RF Transceiver with support for IEEE 802.11 a/b/g/n/ax Wi-Fi6
  - Medium access controller (MAC)
- Hardware-based encryption and decryption using supporting WPA2 and WPA3

- TWT and OFDMA for optimal embedded performance
- Application throughput up to 50 Mbps
- Supports 4-bit SDIO and SPI host interfaces
- Bluetooth® Low Energy 5.2
  - Bluetooth 5.2 supporting long-range and highspeed PHYs (up to 2 Mbps)
  - Host controller interface (HCI) transport for Bluetooth with option for shared SDIO or UART
  - Bluetooth Low Energy certified stack
- Integrated 2.4G-Hz PA for complete wireless solution with up to +20dBm output power
- Security
  - Secured host interface
  - Firmware authentication
  - Anti-rollback protection
- Power Management
  - VDD_1V8: 1.62 V - 1.98 V
  - VDD_3V3: 2.1 V - 4.2 V

- Clock Source:
  - On module 40 MHz XTAL fast clock
  - External 32.768-kHz slow clock by default
- Package
  - 64-QFM, 13.4-mm x 13.3-mm x 2-mm (BDE-BW3351NP1, BDE-BW3351NP2)
  - 64-QFM, 18.4-mm x 13.3-mm x 2-mm (BDE-BW3351UP1, BDE-BW3351UP2)
  - Pin to Pin Compatible with TI's WL1837MOD (BDE-BW3351NP1, BDE-BW3351NP2)
  - Pin to Pin Compatible with BDE's BDE-BW2837 (BDE-BW3351NP1, BDE-BW3351NP2)
- Regulatory (In Progress)
  - FCC
  - IC
  - CE-RED
  - Bluetooth SIG

Applications

- Grid Infrastructure
  - Electricity Meter
  - String Inverter
  - Micro Inverter
  - Energy Storage Power Conversion System (PCS)
- Building and Home Automation
  - HVAC Controller
  - HVAC Gateway
  - Thermostat
  - Building Security Gateway
  - Garage door system
  - IP network camera/ Video doorbell
  - Wireless security camera
- Appliances
  - Refrigerator & freezer
  - Oven
  - Washer & dryer
  - Residential water heater & heating system

- Air purifier & humidifier
- Coffee machine
- Air conditioner indoor unit
- Vacuum robot
- Robotic lawn mower
- Medical
  - Infusion pump
  - Electronic hospital bed & bed control
  - Multiparameter patient monitor
  - Blood glucose monitor
  - Blood pressure monitor
  - CPAP machine
  - Telehealth systems
  - MRI
  - Ultrasound scanner
  - Ultrasound smart probe
  - Electric toothbrush
- Retail Automation and Payment

Contents

1. References

TBD

2. Block Diagram

BDE-BW3351xPx module is based on the TI's 10th generation connectivity combo chip CC3351.

The module, as seen in below diagrams, depending on different configurations, comprises of:

- 40-MHz XTAL

- Bandpass filter

- Decoupling capacitors

- RF switch (BDE-BW3351NP2, BDE-BW3351UP2)
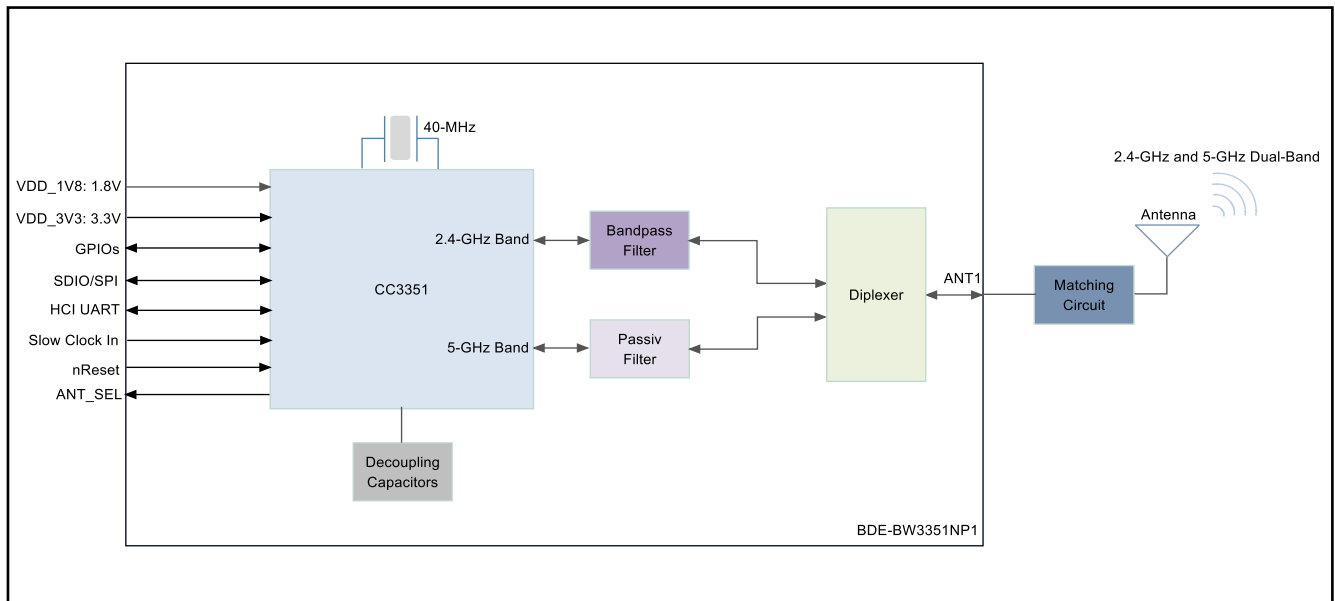
- U.FL connector (BDE-BW3351UP1, BDE-BW3351UP2)

Figure 2-1. Block Diagram of BDE-BW3351NP1
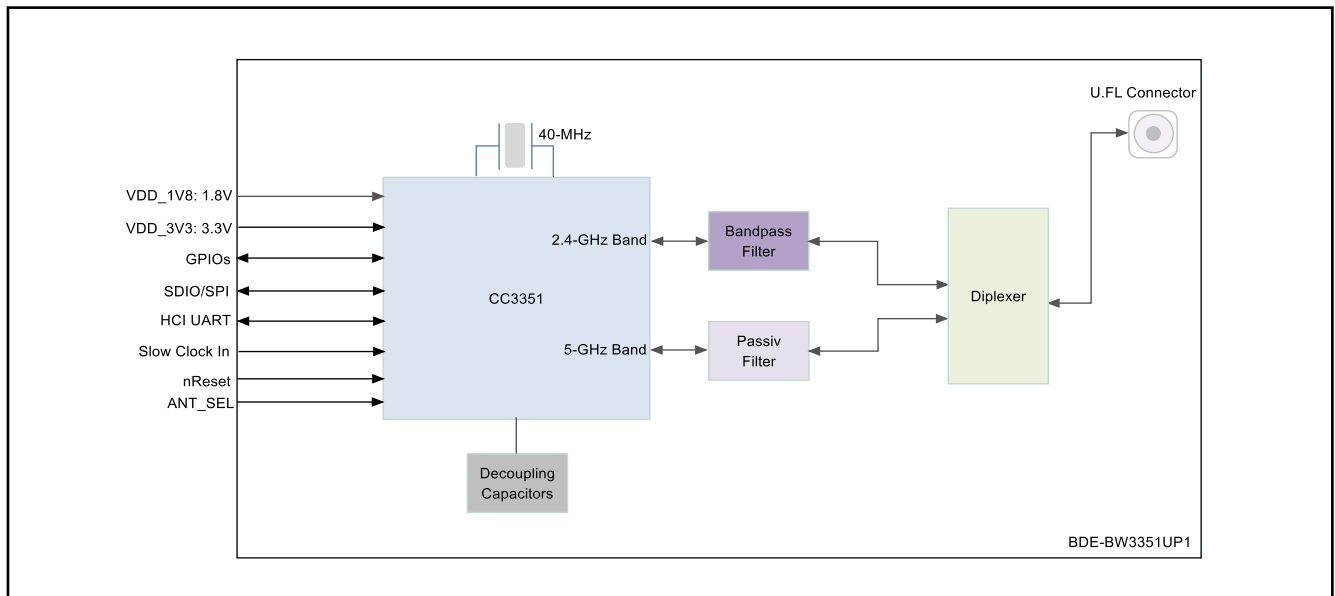
Figure 2-2. Block Diagram of BDE-BW3351UP1
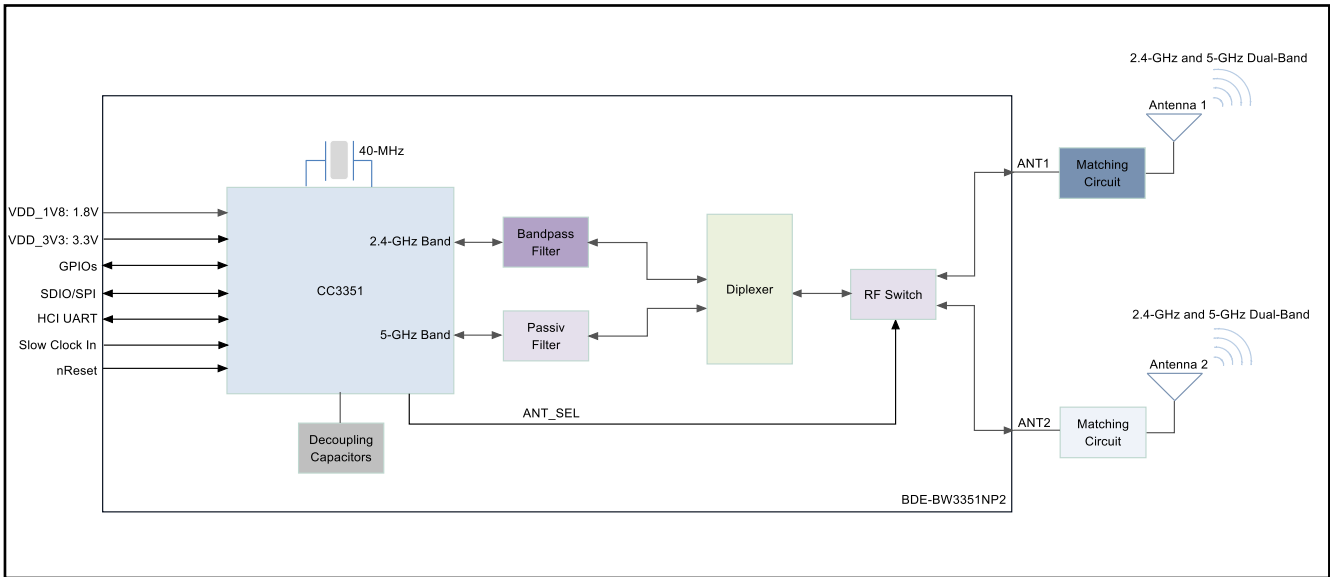
Figure 2-3. Block Diagram of BDE-BW3351NP2
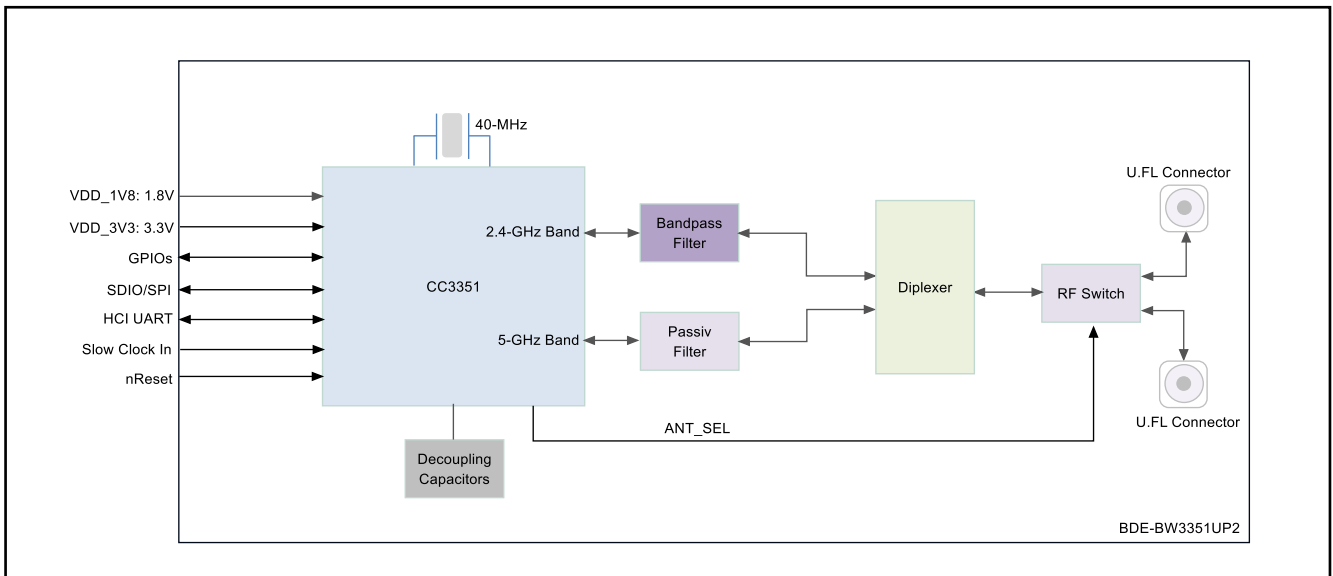
Figure 2-4. Block Diagram of BDE-BW3351UP2

3. Terminal Configuration and Functions

3.1. Pin Diagram
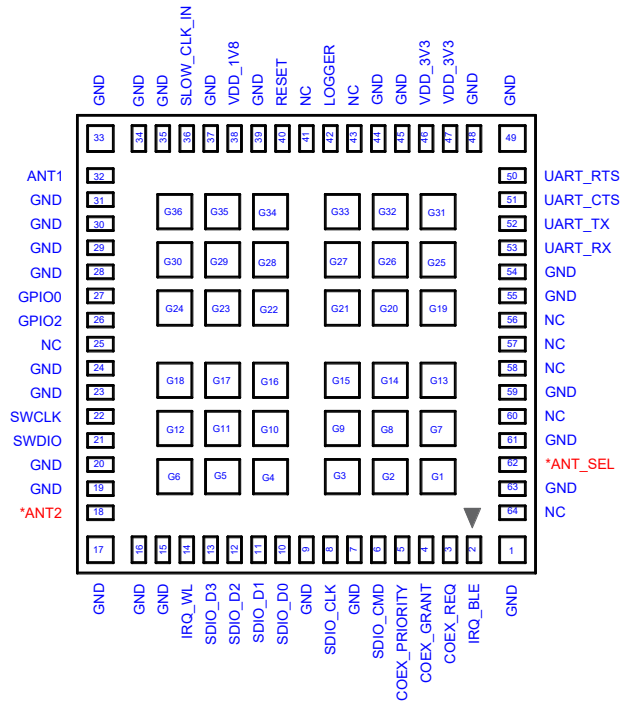
Notes:

Pin ANT2 is only for BDE-BW3351NP2;

1. Pin ANT_SEL is only for BDE-BW3351NP1;

Figure 3-1. Pin Diagram of BDE-BW3351NP1 and BDE-BW3351NP2 (Bottom View)

Notes:

1. Pin ANT_SEL is only for BDE-BW3351UP1;

Figure 3-2. Pin Diagram of BDE-BW3351UP1, BDE-BW3351UP2 (Bottom View)

3.2. Pin Attributes and Pin Multiplexing

Table 3-1. Pin Description

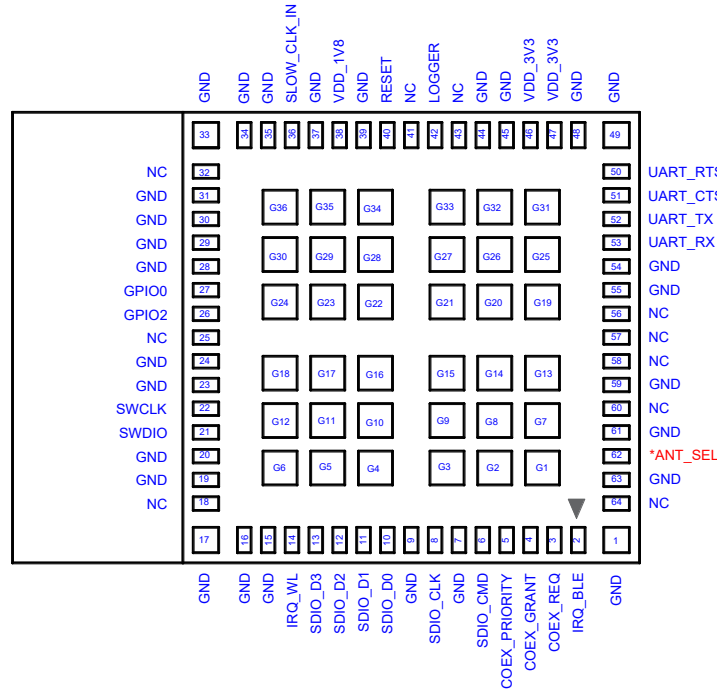| Module Pin #	Pin Name	Type	Description
1	GND	Ground	Power ground
2	IRQ_BLE	O	IRQ_BLE to Host (in shared SDIO mode)
3	COEX_REQ	I	External Coexistence Interface – Request
4	COEX_GRANT	O	External Coexistence Interface – Grant
5	COEX_PRIORITY	I	External Coexistence Interface – Priority
6	SDIO_CMD	I	SDIO_CMD_WL (SPI_DIN)
7	GND	Ground	Power ground
8	SDIO_CLK	I	SDIO_CLK_WL (SPI_CLK). Must be driven by host
9	GND	Ground	Power ground
10	SDIO_D0	I/O	SDIO_D0_WL (SPI_DOUT)
11	SDIO_D1	I/O	SDIO_D1_WL
12	SDIO_D2	I/O	SDIO_D2_WL
13	SDIO_D3	I/O	SDIO_D3_WL (SPI_CSX)
14	IRQ_WL	O	IRQ_WL to Host
15	GND	Ground	Power ground
16	GND	Ground	Power ground
17	GND	Ground	Power ground
18	ANT2	ANT2	Secondary antenna for antenna diversity Only for BDE-BW3351NP2, BDE-BW3351UP2
	NC	-	No Connect for BDE-BW3351NP1, BDE-BDE-BW3351UP1
19	GND	Ground	Power ground
20	GND	Ground	Power ground
21	SWDIO	I/O	Serial Wire DIN/DOUT
22	SWCLK	I	Serial Wire CLK
23	GND	Ground	Power ground
24	GND	Ground	Power ground
25	NC	-	No Connect
26	GPIO2	I/O	GPIO
27	GPIO0	I/O	GPIO
28	GND	Ground	Power ground
29	GND	Ground	Power ground
30	GND	Ground	Power ground
31	GND	Ground	Power ground
32	ANT1	ANA	Bluetooth Low Energy and WLAN 2.4-GHz RF Port
33	GND	Ground	Power ground
34	GND	Ground	Power ground
35	GND	Ground	Power ground
36	SLOW_CLK_IN	I	External Slow Clock Input
37	GND	Ground	Power ground
38	VDD_1V8	Power	1.8V Power supply
39	GND	Ground	Power ground
40	RESET	I	Reset
41	NC	-	No Connect
42	LOGGER	O	Tracer (UART TX Debug Logger)
43	NC	-	No Connect
44	GND	Ground	Power ground

45	GND	Ground	Power ground
46	VDD_3V3	Power	3.3V Power supply
47	VDD_3V3	Power	3.3V Power supply
48	GND	Ground	Power ground
49	GND	Ground	Power ground
50	UART_RTS	O	UART RTS for Flow Control for Bluetooth Low Energy HCI
51	UART_CTS	I	UART CTS for flow control for BLE HCI
52	UART_TX	O	UART TX for BLE HCI
53	UART_RX	I	UART RX for BLE HCI
54	GND	Ground	Power ground
55	GND	Ground	Power ground
56	NC	-	No Connect
57	NC	-	No Connect
58	NC	-	No Connect
59	GND	Ground	Power ground
60	NC	-	No Connect
61	GND	Ground	Power ground
62	ANT_SEL	O	Antenna select control for antenna diversity, only for BDE-BW3351NP1, BDE-BDE-BW3351UP1
	NC	-	No connect for BDE-BW3351NP2, BDE-BW3351UP2
63	GND	Ground	Power ground
64	NC	-	No Connect
G1 – G36	GND	Ground	Power ground, thermal pads

4. Specifications

4.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PARAMETER	MIN	MAX	UNIT	Notes
V_{DD_3V3}	TBD	TBD	V	
V_{DD_1V8}	TBD	TBD	V	
RF pin	TBD	TBD	dBm	
Storage Temperature	TBD	TBD	°C	

4.2. ESD Ratings

		VALUE	UNIT
V (ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	TBD	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
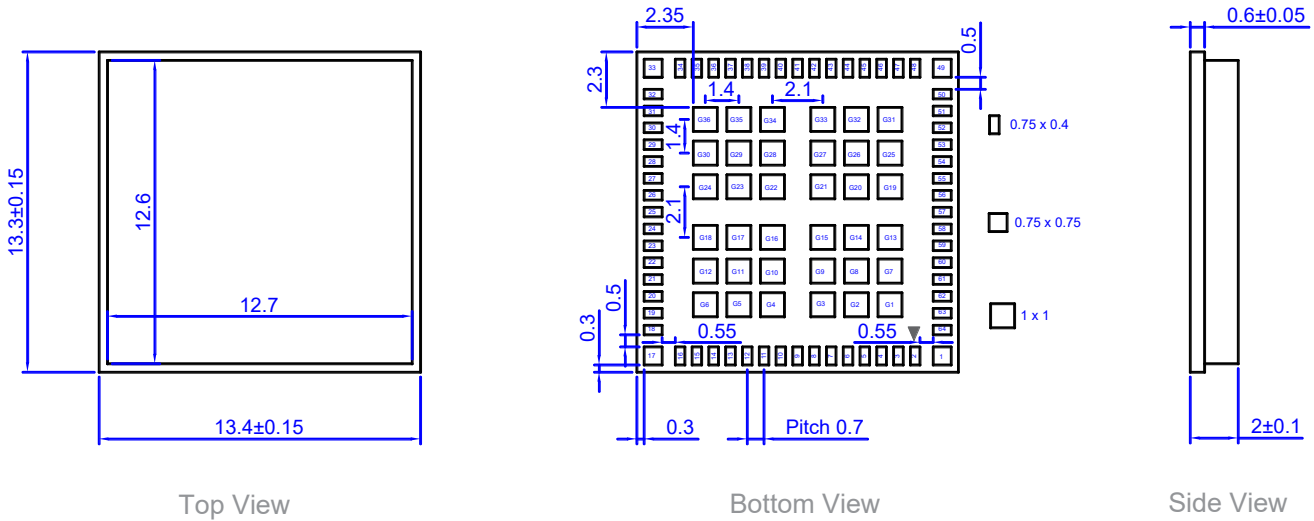
4.3 Recommended Operating Conditions

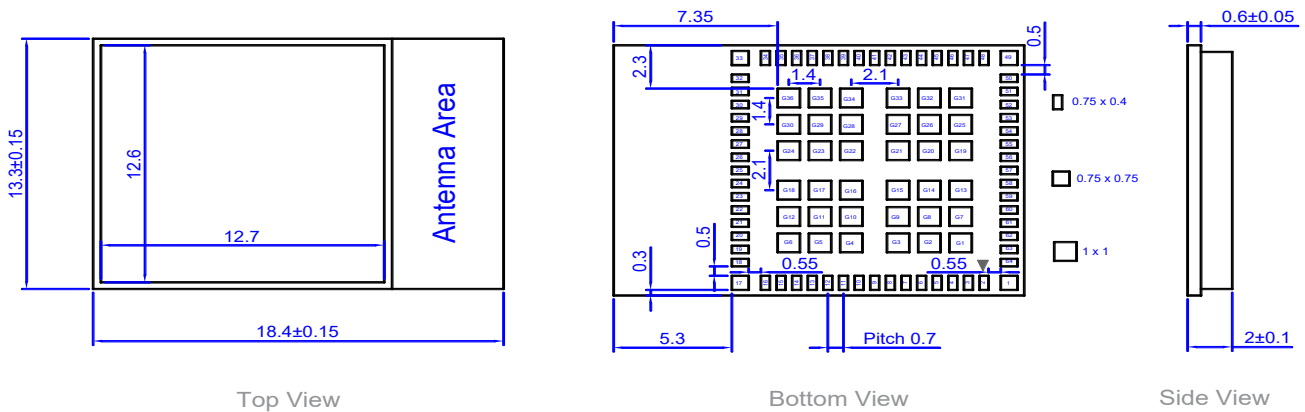| PARAMETER	MIN	TYP	MAX	UNIT	Notes
V_{DD_3V3}	2.1	3.3	4.2	V	
V_{DD_1V8}	1.62	1.8	1.98	V	
Storage Temperature	-40		85	°C	

5. Mechanical Specifications

5.1 Dimensions

Fig 5-1 and Fig 5-2 show the overall dimensions of the modules.

Note: All dimensions are in mm.
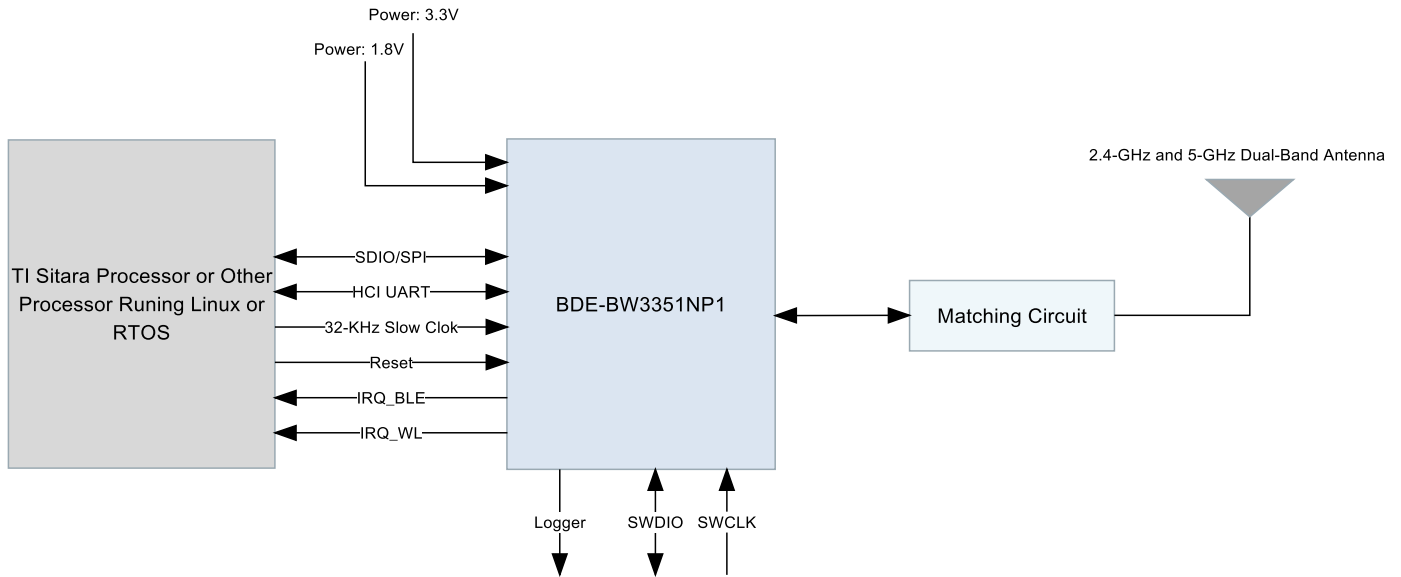
Top View   Bottom View   Side View

Figure 5-1. Mechanical Drawing of BDE-BW3351NP1 and BDE-BW3351NP2

Top View   Bottom View   Side View

Figure 5-2. Mechanical Drawing of BDE-BW3351UP1, BDE-BW3351UP2

6. Reference Design

6.1 Block Diagram

Figure 6-1. High-Level System Block Diagram

Note: Pin IRQ_BLE, IRQ_WL and Logger are assigned as the SoP mode pins, the default SoP mode is "001", which is IRQ_BLE pin being pulled down, IRQ_WL pin being pulled down and Logger pin being pulled up by default.

6.2 Reference Schematic

For reference schematic, please refer to the design files of BDE-EVM-3351NP.

6.3 Design Consideration

ITEM	DESCRIPTION
Thermal	
1	The proximity of ground vias must be close to the pad.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	

7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (Coplanar or microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
Supply and Interface	
14	The power trace for VBAT must be at least 40-mil wide.
15	The 1.8-V trace must be at least 18-mil wide.
16	Make VDD_3V3 and VDD_1V8 traces as wide as possible to ensure reduced inductance and trace resistance.
17	If possible, shield 3V3 and 1V8 traces with ground above, below, and beside the traces.
18	SDIO signals traces (CLK, CMD, DO, 01, 02, and 03) must be routed in parallel to each other and as short as possible (less than 12 cm). In addition, every trace length must be the same as the others. There should be enough space between traces- greater than 1.5 times the trace width or ground- to ensure signal quality, especially for the SDIO_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. BDE recommends adding ground shielding around these buses.
19	SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

7. Ordering Information

Part Number	Description	Size (mm)	Core Chip	Shipping Form	MOQ
BDE-BW3351NP1	Single antenna port without antenna	13.4 x 13.3 x 2	CC3351	Tape & Reel	1K
BDE-BW3351UP1	Single antenna port with U.FL connector	18.4 x 13.3 x 2	CC3351	Tape & Reel	1K
BDE-BW3351NP2	Dual antenna ports with antenna diversity without antenna	13.4 x 13.3 x 2	CC3351	Tape & Reel	1K
BDE-BW3351UP2	Dual antenna ports with antenna diversity with integrated U.FL connector	18.4 x 13.3 x 2	CC3351	Tape & Reel	1K

8. Revision History

Revision	Date	Description
V0.1	25-July-2023	Preliminary, draft

You can find the latest documentation in this Link.

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