General Description

BDE-WF3135N dramatically simplifies the implementation of Internet connectivity. This dual-band Wi-Fi® network processor module can be added to any low-cost, low-power microcontroller unit (MCU); it integrates all protocols for Wi-Fi® and Internet, which greatly minimize host MCU software requirements.
This ROM-based subsystem includes an 802.11 a/b/g/n dual-band 2.4 GHz and 5 GHz radio, baseband, and MAC with powerful hardware cryptographic engine. With built-in security protocols, the BDE-WF3135N solution provides a robust and simple security experience. The BDE-WF3135N is available in an LGA package that is easy to lay out with all required components including serial Flash, RF filters, diplexer, crystal, and passive components that are fully integrated.

This generation introduces new capabilities that further simplify the connectivity of things to the Internet. The main new features of BDE-WF3135N include:

- 802.11 a/b/g/n: 2.4 GHz and 5 GHz support
- 2.4 GHz Coexistence with Bluetooth® low energy radio
- Antenna diversity
- More concurrent secure sockets, up to 16
- Unique device identifier with ability to generate certificate signing request (CSR)
- Online certificate status protocol (OCSP)
- Wi-Fi Alliance® certified for IoT low power capabilities
- Hostless mode for offloading template packet transmissions
- Improved fast scan.

Key Features

- Fully integrated and green/RoHS module includes all required clocks, serial peripheral interface (SPI) flash, and passives
- Integrated Wi-Fi® and internet protocols
- 802.11a/b/g/n: 2.4 GHz and 5 GHz
- Rich set of IoT security features helps developers protect data
- Low-power modes for battery powered application
- Coexistence with 2.4 GHz radios
- Industrial temperature: –40°C to +85°C
- Wi-Fi network processor subsystem:
  - Wi-Fi core:
    - 802.11 a/b/g/n 2.4 GHz and 5 GHz
    - Modes:
      - Access Point (AP)
      - Station (STA)
      - Wi-Fi Direct® (only supported 2.4 GHz)
    - Security:
      - WEP
      - WPA™/ WPA2™ PSK
      - WPA2 Enterprise
      - WPA3™ Personal
  - Internet and application protocols:
    - HTTPs server, mDNS, DNS-SD, DHCP
    - IPv4 and IPv6 TCP/IP stack
    - 16 BSD sockets (fully secured TLS v1.2 and SSL 3.0)
  - Built-in power management
  - subsystem:
    - Configurable low-power profiles (always on, intermittently connected, tag)
    - Advanced low-power modes
    - Integrated DC/DC regulators

- Application throughput
  - UDP: 16 Mbps
  - TCP : 13 Mbps
- Multilayered Security Features:
  - Separate execution environments
  - Networking security
  - Device identity and key
  - Hardware accelerator cryptographic engines (AES, DES, SHA/MD5, CRC)
  - File system security (encryption, authentication, access control)
  - Initial secure programming
  - Software tamper detection
  - Secure boot
  - Certificate signing request (CSR)
  - Unique per device key pair
- Recovery mechanism – ability to recover to factory defaults
- Power-Management Subsystem:
  - Integrated DC/DC converters support a wide range of supply voltage:
    - Single wide-voltage supply, VBAT: 2.3 V to 3.6 V
  - Advanced low-power modes:
    - Shutdown: 1 µA hibernate: 5.5 µA
    - Low-power deep sleep (LPDS): 115 µA
    - Idle connected (MCU in LPDS): 710 µA
    - RX traffic (MCU active): 53 mA
    - TX traffic (MCU active): 223 mA
- Wi-Fi TX power
  - 2.4 GHz: 16 dBm at 1 DSSS
  - 5 GHz: 15.1 dBm at 6 OFDM
- Wi-Fi RX sensitivity
  - 2.4 GHz: –94.5 dBm at 1 DSSS
  - 5 GHz: –89 dBm at 6 OFDM
- Additional integrated components on module
  - 40.0 MHz crystal with internal oscillator
  - 32.768 kHz crystal (RTC)
  - 32 Mbit SPI Serial Flash
  - RF filters, diplexer, and passive components
- QFM package
  - 1.27-mm pitch, 63-pin, 20.5-mm × 17.5-mm QFM package for easy assembly and low-cost PCB design

Applications

For Internet of Things applications, such as:

- Medical and Healthcare
  - Multiparameter Patient Monitor
  - Electrocardiogram (ECG)
  - Electronic Hospital Bed & Bed Control
  - Telehealth Systems
- Building and Home Automation:
  - HVAC Systems & Thermostat
  - Video Surveillance, Video Doorbells, and Low-Power Camera
  - Building Security Systems and E-locks
- Appliances
- Asset Tracking
- Factory Automation
- Grid Infrastructure

Table 0-1. WF3135 Device Family

Part Number	Core Chip	Description	Size (mm)	Package
BDE-WF3135A	CC3135	With chip antenna	20.5 × 25 × 2.4	SMD-63
BDE-WF3135U	CC3135	With U.FL connector for external antenna	20.5 × 25 × 2.4	SMD-63
BDE-WF3135N	CC3135	Without antenna	20.5 × 17.5 × 2.4	SMD-63

Contents

General Description 1
Key Features 1
Applications 2
Contents 3
1. References 4
2. Block Diagram 5
3. Pinout 7
3.1 Pin Attributes 7
3.2 Signal Descriptions 10
3.3 Connections for Unused Pins 13
4. Characteristics 13
4.1. Absolute Maximum Ratings 13
4.2. Recommended Operating Conditions 14
4.3. Current Consumption Summary: 2.4GHz GF Band 14
4.4. Current Consumption Summary: 5 GHz RF Band 15
4.5. Electrical Characteristics for DIO Pins 16
4.6. BLE and WLAN Coexistence Requirements 17
4.7. Reset Requirement 17
4.8. Thermal Resistance Characteristics for MOB Package 17
4.9. Timing and Switching Characteristics 18
4.10. External Interfaces 20
4.11. Brownout and Blackout Conditions 23
5. Detailed Description 25
5.1 Overview 25
5.2 Module Features 25
5.3 Restoring Factory Default Configuration 29
5.4 Hostless Mode 29
6. Mechanical Specifications 31
6.1 Dimensions 31
7. Application Information 32
7.1 BLE/2.4 GHz Radio Coexistence 32
7.2 Antenna Selection 33
7.3 Typical Application 34
7.4 Power Supply Decoupling and Bulk Capacitors 35
7.5 Reset 35
7.6 Unused Pins 35
8. Ordering Information 36
9. Regulatory Information 36
Revision History 36

1. References

[1] CC3135 resources: https://www.ti.com/product/CC3135

2. Block Diagram

Figure 1 shows the functional block diagram of the BDE-WF3135N module.

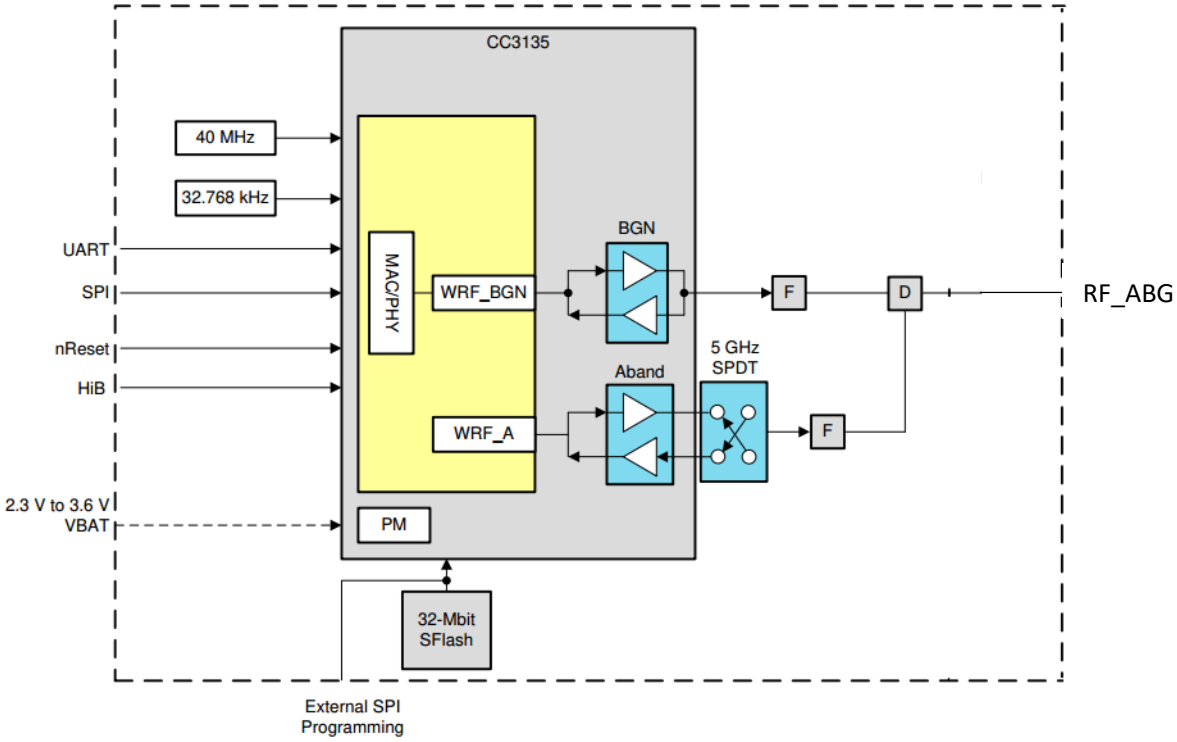

Figure 1. BDE-WF3135N Module Block Diagram

Figure 2 shows the CC3135 hardware overview.

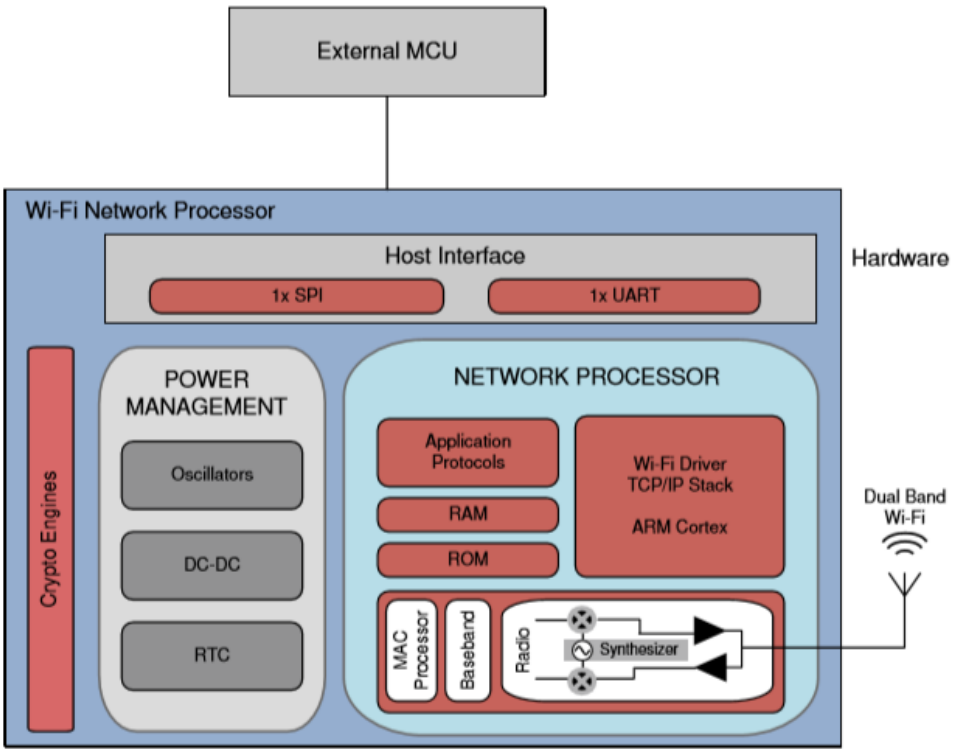

Figure 2. CC3135 Hardware Overview

Figure 3 shows an overview of the CC3135 embedded software.

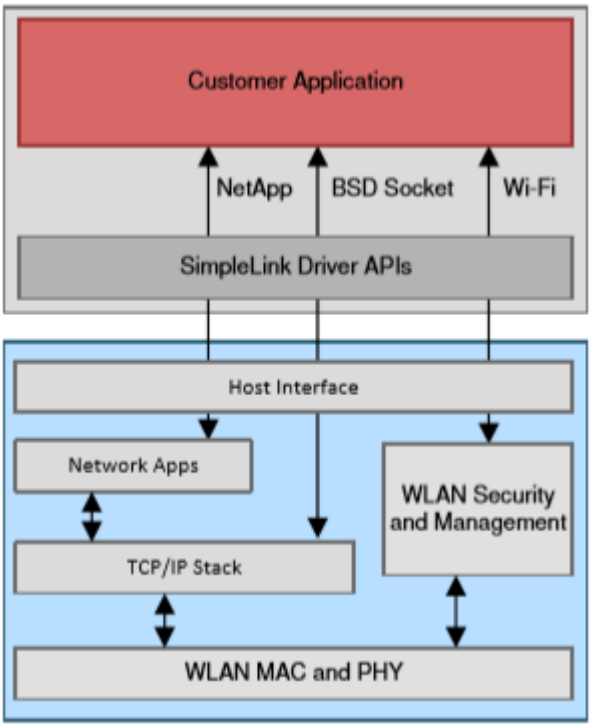

Figure 3. CC3135 Embedded Software

3. Pinout

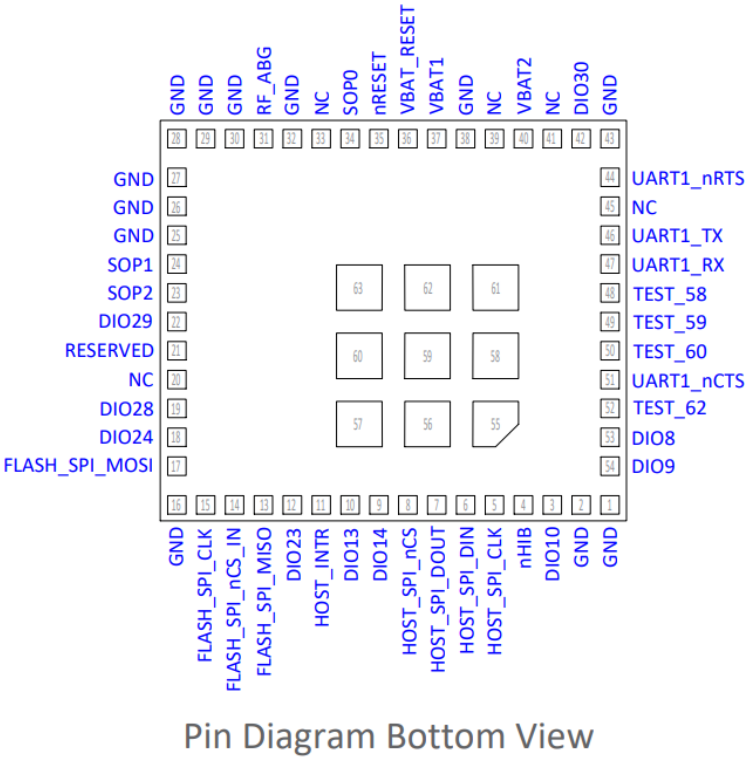

Figure 4. Pin Diagram Bottom View

3.1 Pin Attributes

Table 3-1 describes the BDE-WF3135N pins.

Table 3-1. Pin Description

Pin #	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
1	GND	–	Power	GND
2	GND	–	Power	GND
3	DIO10	–	I/O	Digital input or output
4	nHIB	Hi-Z	I	Hibernate signal input to the NWP subsystem (active low). This is connected to the MCU GPIO. If the GPIO from the MCU can float while the MCU enters low power, consider adding a pullup resistor on the board to avoid floating.
5	HOST_SPI_CLK	Hi-Z	I	Host interface SPI clock
6	HOST_SPI_MOSI	Hi-Z	I	Host interface SPI data input
7	HOST_SPI_MISO	Hi-Z	O	Host interface SPI data output
8	HOST_SPI_nCS	Hi-Z	I	Host interface SPI chip select (active low)
9	DIO12	–	O	Digital input or output
10	DIO13	–	–	Digital input or output

Pin #	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
11	HOST_INTR	Hi-Z	O	Interrupt output (active high)
12	DIO23	Hi-Z		Digital input or output

Pin #	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
13	FLASH _SPI_MISO	Hi-Z	I	External Serial Flash Programming: SPI data in
14	FLASH _SPI_CS	Hi-Z	O	External Serial Flash Programming: SPI chipselect (active low)
15	FLASH_SPI_CLK	Hi-Z	O	External Serial Flash Programming: SPI clock
16	GND	–	Power	Ground
17	FLASH_SPI_MOSI	Hi-Z	O	External Serial Flash Programming: SPI data out
18	DIO24	Hi-Z		Digital input or output
19	DIO28	–	–	Digital input or output
20	NC	–	–	No Connect
21	Reserved	Hi-Z	–	No Connect
22	DIO29	Hi-Z		Digital input or output
23	SOP2	Hi-Z	O	A 100 kΩ pull down resistor is internally tied to this SOP pin.
24	SOP1	Hi-Z	–	A 100 kΩ pull down resistor is internally tied to this SOP pin. SOP[2:0] used for factory restore.
25	GND	–	Power	GND
26	GND	–	Power	GND
27	GND	–	Power	GND
28	GND	–	Power	GND
29	GND	–	Power	GND
30	GND	–	Power	GND
31	RF_ABG	Hi-Z	RF	2.4 GHz & 5 GHz RF TX, RX
32	GND	–	Power	GND
33	NC	–	–	No Connect
34	SOP0	Hi-Z	–	A 100 kΩ pull down resistor is internally tied to this SOP pin. SOP[2:0] used for factory restore.
35	nRESET	Hi-Z	I	There is an internal 100 kΩ pull-up resistor option from the nRESET pin to VBAT_RESET. Note: VBAT_RESET is not connected to VBAT1 or VBAT2 within the module. The following connection schemes are recommended: • Connect nRESET to a GPIO from the host only if nRESET will be in a defined state under all operating conditions. Leave VBAT_RESET unconnected to save power. • If nRESET cannot be in a defined state under all operating conditions, connect VBAT_RESET to the main module power supply (VBAT1 and VBAT2). Due to the internal pull-up resistor, a leakage current of 3.3 V / 100 kΩ is expected.
36	VBAT_RESET	Hi-Z	–	
37	VBAT1	Hi-Z	-	Power supply for the module, must be connected to battery (2.3 V to 3.6 V)
38	GND	–	Power	GND
39	NC	–	–	No Connect
40	VBAT2	Hi-Z	-	Power supply for the module, must be connected to battery (2.3 V to 3.6 V)
41	NC	–	–	No Connect
42	DIO30	Hi-Z	–	Network Scripter I/O

Pin #	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
43	GND	–	Power	GND
44	UART1_nRTS	Hi-Z	O	UART interface to host (request to send)
45	NC	–	–	No Connect
46	UART1_TX	Hi-Z	O	UART interface to host (transmit)

Pin #	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
47	UART1_RX	Hi-Z	I	UART interface to host (receive)
48	TEST_58	Hi-Z	O	Test signal; connect to an external test point.
49	TEST_59	Hi-Z	O	Test signal; connect to an external test point.
50	TEST_60	Hi-Z	O	Test signal; connect to an external test point.
51	UART1_nCTS	Hi-Z	I	UART interface to host (clear to send)
52	TEST_62	Hi-Z	O	Test signal; connect to an external test point.
53	DIO8	Hi-Z		Digital input or output
54	DIO9	Hi-Z	–	Digital input or output

(1) I = input, O = output, RF = radio frequency, I/O = bidirectional

3.2 Signal Descriptions

Table 3-2: Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Antenna selection	DIO10	3	I/O	O	Antenna selection control
	DIO12	9	I/O	O	
	DIO13	10	I/O	O	
	DIO23	12	I/O	O	
	DIO24	18	I/O	O	
	DIO28	19 (1)	I/O	O	
	DIO29	22	I/O	O	
	DIO25	23	O	O	
	DIO30	42(1)	I/O	O	
	DIO3	48	I/O	O	
	DIO4	49	I/O	O	
	DIO5	50	I/O	O	
	DIO8	53	I/O	O	
	DIO9	54	I/O	O	
BLE/2.4 GHz Radio coexistence(2)	DIO10	3	I/O	I/O	Coexistence inputs and outputs
	DIO12	9	I/O	I/O	
	DIO13	10	I/O	I/O	
	DIO23	12	I/O	I/O	
	DIO24	18	I/O	I/O	
	DIO28	19 (1)	I/O	I/O	
	DIO29	22	I/O	I/O	
	DIO30	42 (1)	I/O	I/O	
	DIO3	48	I/O	I/O	
	DIO4	49	I/O	I/O	
	DIO5	50	I/O	I/O	
	DIO8	53	I/O	I/O	
	DIO9	54	I/O	I/O	
Hostless Mode	DIO10	3	I/O	I/O	Hostless mode inputs and outputs
	DIO12	9	I/O	I/O	
	DIO13	10	I/O	I/O	
	DIO23	12	I/O	I/O	
	DIO24	18	I/O	I/O	
	DIO28	19 (1)	I/O	I/O	
	DIO29	22	I/O	I/O	
	DIO25	23	O	O	
	DIO30	42 (1)	I/O	I/O	
	DIO3	48	I/O	I/O	

	DIO4	49	I/O	I/O	
	DIO5	50	I/O	I/O	
	DIO8	53	I/O	I/O	
	DIO9	54	I/O	I/O	

Table3-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
HOST SPI	HOST_SPI_CLK	5	I/O	I	Host SPI clock input
	HOST_SPI_MOSI	6	I/O	I	Data from Host
	HOST_SPI_MISO	7	I/O	O	Data to Host
	HOST_SPI_nCS	8	I/O	I	Device select (active low)
FLASH SPI	FLASH_SPI_DIN	13	I	I	External serial Flash interface: SPI data in
	FLASH_SPI_CS	14	O	O	External serial Flash interface: SPI chip select (active low)
	FLASH_SPI_CLK	15	O	O	External serial Flash interface: SPI clock
	FLASH_SPI_MOSI	17	O	O	External serial Flash interface: SPI dta out
UART	UART1_nRTS	44	I/O	O	UART1 request-to-send (active low)
	UART1_TX	46	I/O	I	UART TX data
	UART1_RX	47	I/O	O	UART RX data
	UART1_nCTS	51	I/O	I	UART1 clear-to-send (active low)
Sense-On-Power	SOP2	23 (3)	O	I	Sense-on-power 2
	SOP1	24	I	I	Configuration sense-on-power 1
	SOP0	34	I	I	Configuration sense-on-power 0
Power	VBAT1	37	-	-	Power supply for the module
	VBAT2	40	-	-	Power supply for the module
nHIB	nHIB	4	I	I	Hibernate signal input to the NWP subsystem (active low)
RF	RF_ABG	31	NC	NC	WLAN analog RF 802.11 a/b/g/n bands
Test Port	TEST_58	48	O	O	Test Signal
	TEST_59	49	I	I	Test Signal
	TEST_60	50	O	O	Test Signal
	TEST_62	52	O	O	Test Signal

(1) LPDS retention unavailable.

(2) The BDE-WF3135N are compatible with TI BLE modules using an external RF switch.

(3) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

3.3 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. Table 3-3 provides a list of NC pins.

Table3-3. Connections for Unused Pins

FUNCTION	SIGNAL DESCRIPTION	PIN NUMBER	ACCEPTABLE PRACTICE
DIO	Digital input or output	3, 9, 10, 12, 18, 19, 22, 42, 53, 54	Wake up I/O source should not be floating during hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused GPIOs as NC
No Connect	NC	20, 21, 31,33, 39, 41, 45	Unused pin, leave as NC.
SOP	Configuration sense-on-power	23, 24, 34	Leave as NC (Modules contain internal 100 kΩ pull down resistors on the SOP lines). An external 10 kΩ pull up resistor is required for factory restore.
Reset	RESET input for the device	35, 36	There is an internal 100 kΩ pull-up resistor option from the nRESET pin to VBAT_RESET. Note: VBAT_RESET is not connected to VBAT1 or VBAT2 within the module. The following connection schemes are recommended: • Connect nRESET to a GPIO from the host only if nRESET will be in a defined state under all operating conditions. Leave VBAT_RESET unconnected to save power. • If nRESET cannot be in a defined state under all operating conditions, connect VBAT_RESET to the main module power supply (VBAT1 and VBAT2). Due to the internal pull-up resistor, a leakage current of 3.3 V / 100 kΩ is expected.

4. Characteristics

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only.
Default measurement conditions (unless otherwise specified): VBAT= 3.0 V, TA = 25 ℃. All radio measurements are performed with standard RF measurement equipment.

4.1. Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the module can occur. Functional operation is not ensured under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the module (1)(2).

Table 4-1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{BAT}	–0.5	3.8	V
Digital I/O	–0.5	VBAT + 0.5	V
RF pin	–0.5	2.1	V

Parameter	Min	Max	Unit
Analog pins	–0.5	2.1	V
Operating temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–40	85	°C
Junction temperature, T_j (3)		120	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to VSS, unless otherwise noted.

(3) Junction temperature is for the CC3135RNMARGK device that is contained within the module.

4.2. Recommended Operating Conditions

Function operation is not ensured outside this limit, and operation outside this limit for extended periods can adversely affect long-term reliability of the module(1)(2)(3).

Table 4-2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{BAT}	2.3	3.3	3.6	V
Operating temperature	–40	25	85	°C
Ambient thermal slew	–20		20	°C/minute

(1) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.

(2) To ensure WLAN performance, ripple on the 2.3-V to 3.6-V supply must be less than ±300 mV.

(3) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is 2.1 V, and care must be taken when operating at the minimum specified voltage.

4.3. Current Consumption Summary: 2.4GHz GF Band

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS(1)(2)		MIN	TYP	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX(3)	1 DSSS			53		mA
	54 OFDM			53		
Idle connected(4)				690		µA
LPDS				115		µA
Hibernate				5.5		µA
Shutdown				1		µA
Peak calibration current(3)(5)	VBAT = 3.6 V			420		mA
	VBAT = 3.3 V			450		
	VBAT = 2.3 V			610		

(1) TX power level = 0 implies maximum power. TX power level = 4 implies output power backed off approximately 4 dB.

(2) The BDE-WF3135N system is a constant power-source system. The active current numbers scale based on the VBAT voltage supplied.

(3) The RX current is measured with a 1-Mbps throughput rate.

(4) DTIM = 1

(5) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event.

4.4. Current Consumption Summary: 5 GHz RF Band

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
TX	6 OFDM		318		mA
	54 OFDM		293		
RX(3)	54 OFDM		61		mA
Idle connected(4)			690		µA
LPDS			115		µA
Hibernate			5.5		µA
Shutdown			1		µA
Peak calibration current(5) (3)	VBAT = 3.6 V		290		mA
	VBAT = 3.3 V		310		
	VBAT = 2.7 V		310		
	VBAT = 2.3 V		365		

(1) TX power level = 0 implies maximum power. TX power level = 4 implies output power backed off approximately 4 dB.

(2) The BDE-WF3135N system is a constant power-source system. The active current numbers scale based on the VBAT voltage supplied.

(3) The RX current is measured with a 1-Mbps throughput rate.

(4) DTIM = 1

(5) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event.

4.5. Electrical Characteristics for DIO Pins

T_A = 25°C, V_{BAT} = 3.3 V

PARAMETER			TEST CONDITIONS(1)	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × VDD		VDD + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × VDD	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ VDD < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ VDD < 3.6 V			V_{DD} × 0.7	V
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ VDD < 3.6 V			V_{DD} × 0.7	V
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ VDD < 2.4 V			V_{DD} × 0.75	V
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ VDD < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ VDD < 3.6 V	V_{DD} × 0.2			V
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ VDD < 3.6 V	V_{DD} × 0.2			V
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ VDD < 2.4 V	V_{DD} × 0.25			V
I_{OH}	High-level source current	2-mA drive			2		mA
		4-mA drive			4		
		6-mA drive			6		
I_{OL}	Low-level sink current	2-mA drive			2		mA
		4-mA drive			4		
		6-mA drive			6		
V_{IL}	nRESET(2)				0.6		V

(1) We recommend using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

(2) The nRESET pin must be held below 0.6 V for the device to register a reset.

4.6. BLE and WLAN Coexistence Requirements

For proper BLE and WLAN 2.4 GHz radio coexistence, the following requirements must be met.

Table 4-7. BLE/WLAN Coex (1) Isolation Requirement

PARAMETER	Band	MIN	TYP	MAX	UNIT
Port-to-port isolation	Dual antenna configuration(2)	20(3)			dB

(1) The BDE-WF3135N are compatible with TI BLE modules using an external RF switch.
(2) A single antenna configuration is possible using the CC3x35 devices.
(3) For dual antenna configuration antenna placement must be such that isolation between the BLE and WLAN ports is at least 20 dB.

4.7. Reset Requirement

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	Operation mode level		0.65 × V_{BAT}		V
V_{IL}	Shutdown mode level(1)	0	0.6		V
	Minimum time for nReset low for resetting the module	5			ms
T_r and T_f	Rise and fall times		20		µs

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

4.8. Thermal Resistance Characteristics for MOB Package

NO.	PARAMETER	DESCRIPTION	°C/W(1)(2)	AIR FLOW (m/s) (3)
T1	$R\Theta_{JC}$	Junction-to-case	11.4	N/A
T2	$R\Theta_{JB}$	Junction-to-board	8.0	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	19.1	0
T4		Junction-to-moving air	14.7	1
T5			13.4	2
T6			12.5	3
T7	Ψ_{JT}	Junction-to-free air	5.4	0
T8		Junction-to-package top	5.8	1
T9			6.1	2
T10			6.5	3
T11	Ψ_{JB}	Junction-to-free air	6.8	0
T12		Junction-to-board	6.6	1
T13			6.6	2
T14			6.5	3

(1) °C/W = degrees Celsius per watt.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

(3) m/s = meters per second.

4.9. Timing and Switching Characteristics

4.9.1 Power-Up Sequencing

For proper start-up of the BDE-WF3135N module, perform the recommended power-up sequencing as follows:

1. Tie VBAT1 (pin 37) and VBAT2 (pin 40) together on the board.
2. Hold the nRESET pin low while the supplies are ramping up.

Figure 5 shows the reset timing diagram for the first-time power-up and reset removal.

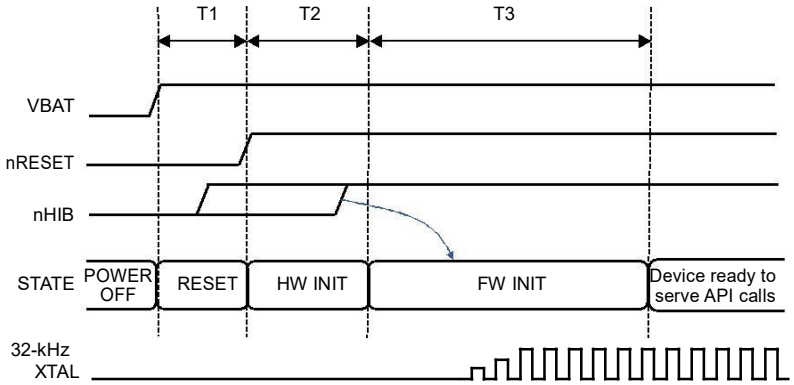

Figure 5. First-Time Power-Up and Reset Removal Timing Diagram

Table 4-8 describes the timing requirements for the first-time power-up and reset removal.

Table 4-8. First-Time Power-Up and Reset Removal Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	nReset time	nReset timing after VBAT supplies are stable		1		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	Internal 32-kHz XTAL settling plus firmware initialization time plus radio calibration		1.35		s

4.9.2 Power-Down Sequencing

For proper power down of the BDE-WF3135N, ensure that the nRESET (pin 35) and nHIB (pin 4) pins have remained in a known state for a minimum of 200 ms before removing power from the module.

4.9.3 Device Reset

When a device restart is required, the user may issue a negative pulse on either the nHIB pin (pin 4) or on the nRESET pin (pin 35), keeping the other pulled high, depending on the configuration of the platform. If the nRESET pin is used, the user must insure the following:

• A high-to-low reset pulse (on pin 35) of at least 200-ms duration.

To ensure a proper reset sequence, the user must call the sl_stop function prior to toggling the reset.

4.9.4 Wakeup From HIBERNATE Mode Timing

Figure 6 shows the timing diagram for wakeup from HIBERNATE mode.

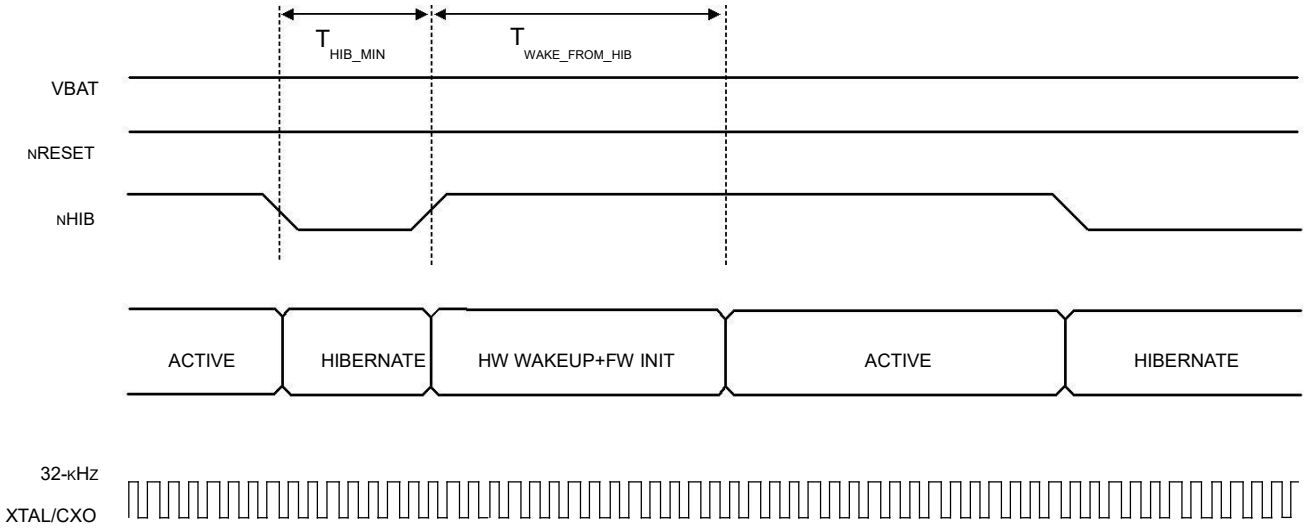

Figure 6. nHIB Timing Diagram

Note

The internal 32.768-kHz XTAL is kept enabled by default when the chip goes into HIBERNATE mode in response to nHIB being pulled low.

Table 4-9 describes the timing requirements for nHIB.

Table 4-9. nHIB Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{hib_min}	Minimum hibernate time	Minimum pulse width of nHIB being low(1)	10			ms
$T_{wake_from_hib}$	Hardware wakeup time plus firmware initialization time	See(2)		50		ms

(1) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.

(2) Ensure that the nHIB pulse width is kept above the minimum requirement under all conditions (such as power up, MCU reset, and so on).

4.10. External Interfaces

This section describes the external interfaces supported by the BDE-WF3135N, as follows:
• SPI Host
• Host UART
• External Flash

4.10.1 SPI Host Interface

The device interfaces to an external host using the SPI. The BDE-WF3135N can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.
Figure 7 shows the SPI host interface.

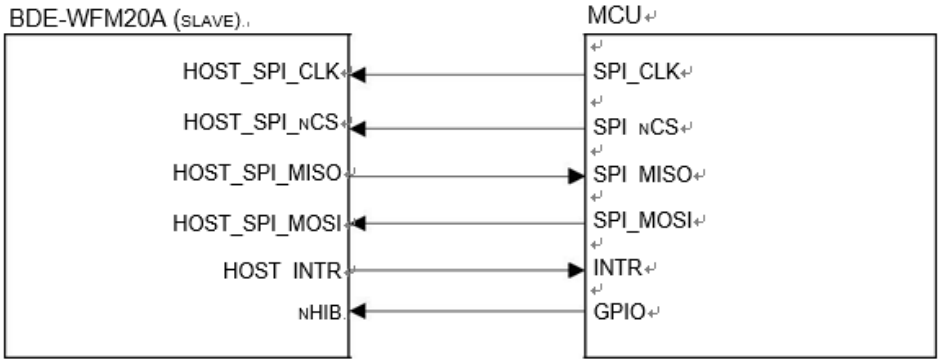

Figure 7. SPI Host Interface

Table 4-10 lists the SPI host interface pins.

Table 4-10. SPI Host Interface

PIN NAME	DESCRIPTION
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to BDE-WF3135N module
HOST_SPI_nCS	CS (active low) signal from MCU host to BDE-WF3135N module
HOST_SPI_MOSI	Data from MCU host to BDE-WF3135N module
HOST_INTR	Interrupt from BDE-WF3135N module to MCU host
HOST_SPI_MISO	Data from BDE-WF3135N module to MCU host
nHIB	Active-low signal that commands the BDE-WF3135N module to enter hibernate mode (lowest power state)

Figure 8 shows the host SPI timing diagram.

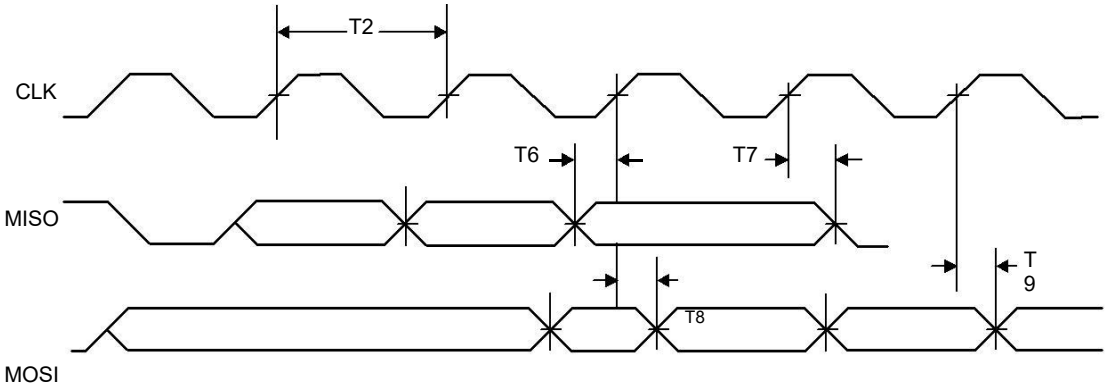

Figure 8. Host SPI Timing

Table 4-11. Host SPI Timing Parameters

PARAMETER NUMBER	DESCRIPTION		MIN	MAX	UNIT
T1	F	Clock frequency at VBAT = 3.3 V		20	MHz
		Clock frequency at VBAT = 2.3 V		12	
T2	t_{clk}	Clock period	50		ns
T3	t_{LP}	Clock low period		25	ns
T4	t_{HT}	Clock high period		25	ns
T5	D	Duty cycle	45%	55%	
T6	t_{IS}	RX data setup time	4		ns
T7	t_{IH}	RX data hold time	4		ns
T8	t_{OD}	TX data output delay		20	ns
T9	t_{OH}	TX data hold time		24	ns

4.10.2 Host UART Interface

The SimpleLink device requires the UART configuration described in Table 4-12.

Table 4-12. UART Configuration

PROPERTY	SUPPORTED CC3135 CONFIGURATION
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	Least significant bit (LSB) first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

4.10.2.1 5-Wire UART Topology

Figure 9 shows the typical 5-wire UART topology comprised of four standard UART lines plus one IRQ line from the device to the host controller to allow efficient low power mode.

Figure 9 shows the typical and recommended UART topology because it offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

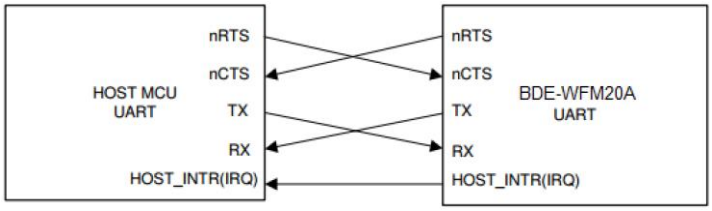

Figure 9. Typical 5-Wire UART Topology

4.10.2.2 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see Figure 10). Using this topology requires one of the following conditions to be met:

- Host is always awake or active.
- Host goes to sleep, but the UART module has receiver start-edge detection for automatic wake up and does not lose data.

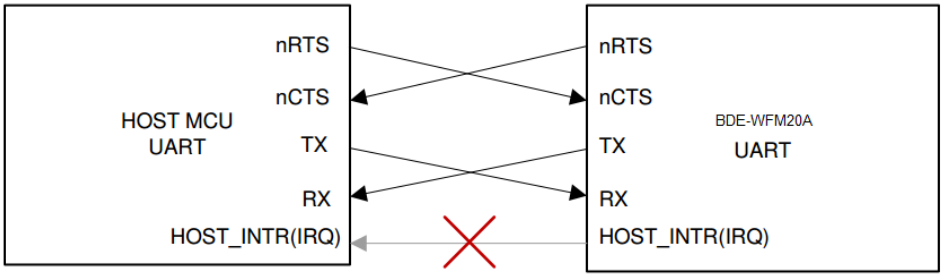

Figure 10. 4-Wire UART Configuration

4.10.2.3 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see Figure 11).

- RX
- TX
- nCTS

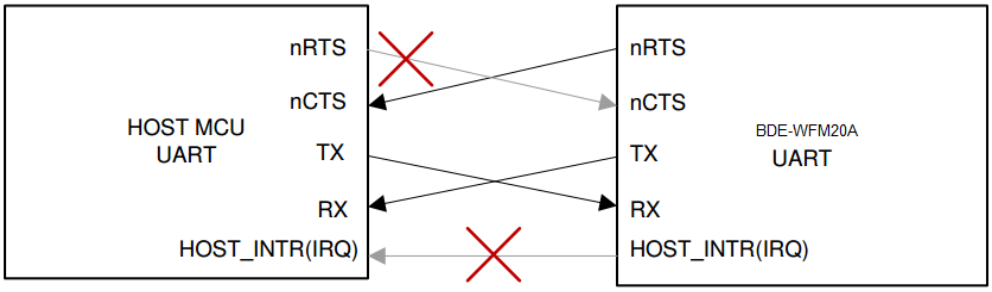

Figure 11. 3-Wire UART Topology

Using 3-wire topology requires one of the following conditions to be met:

- Host always stays awake or active.
- Host goes to sleep, but the UART module has receiver start-edge detection for auto wake up and does not lose data.
- Host can always receive any amount of data transmitted by the SimpleLink device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink device to send its data; thus, the following parameters must be carefully considered:

- Maximum baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

4.10.3 External Flash Interface

The BDE-WF3135N module includes the Macronix 32-Mbit Serial Flash. The Serial Flash can be programmed directly via the external Flash interface (pins 13, 14, 15, and 17). Note that during normal operation, the external Flash interface should remain unconnected.

4.11. Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage dips below VBROWNOUT (see Figure 12 and Figure 13). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (four contacts for a 2× AA battery), and the wiring and PCB routing resistance.

Note

When the device is in the Hibernate state, brownout is not detected; only blackout is in effect during the Hibernate state.

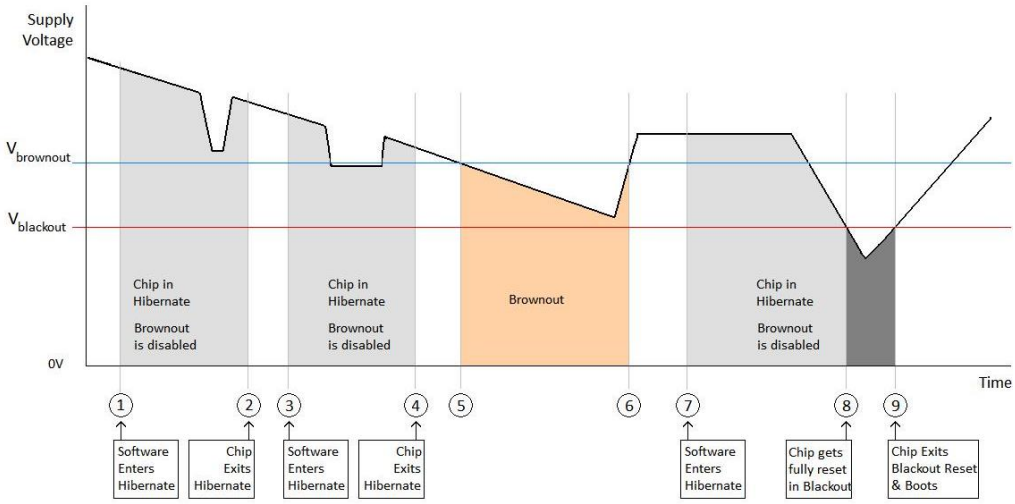

Figure 12. Brownout and Blackout Levels (1 of 2)

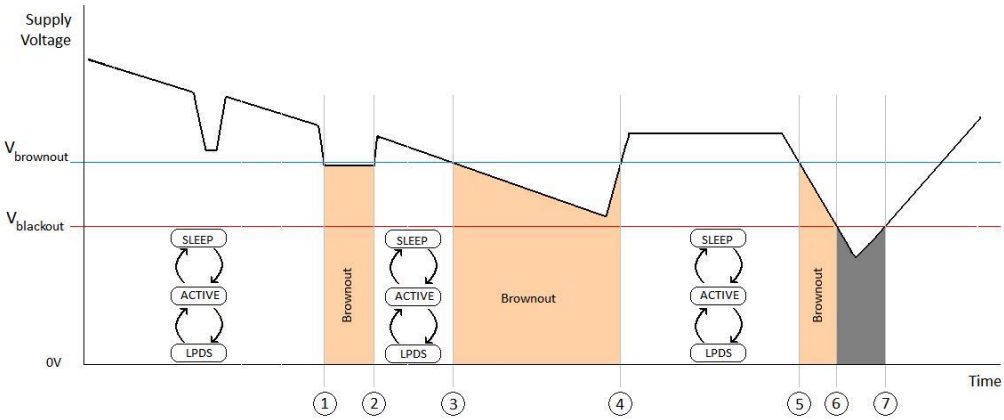

Figure 13. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the CC3135MOD (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 4-13 lists the brownout and blackout voltage levels.

Table 4-13. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

5. Detailed Description

5.1 Overview

The BDE-WF3135N dual-band Wi-Fi module contains a dedicated Arm ® MCU that offloads many of the networking activities from the host MCU. Including an 802.11 a/b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The BDE-WF3135N module supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security, WPS 2.0, and WPA3 personal [11]. The Wi-Fi network processor includes an embedded IPv6 and IPv4 TPC/IP stack.

5.2 Module Features

5.2.1 WLAN

The WLAN features are as follows:

- 802.11 a/b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, and Wi-Fi Direct client and group owner with CCK and OFDM rates in the 2.4 GHz ISM band, channels 1 to 13, and 5 GHz U-NII band.
- Autocalibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in a serial Flash allows automatic, fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks, with on-chip security accelerators, including WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal.
- Smart provisioning options deeply integrated within the device provide a comprehensive end-to-end solution. Elaborate events notification to the host enable the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a BDE-WF3135NMOD-enabled module to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, the device is usable by deeply embedded applications.
- 802.11 transceiver mode transmits and receives proprietary data through a socket without adding MAC or PHY headers, and provides the option to select the working

- channel, rate, and transmitted power. The receiver mode works together with the filtering options.

5.2.2 Network Stack

The network stack features are as follows:

- Integrated IPv4, IPv6, and TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

Note

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, RAW, SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 (Stateful) with DAD and Stateless auto configuration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet
- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial Flash
    - RESTful APIs for setting\configuring application content
    - Dynamic user callbacks
- Service discovery: Multicast DNS service discovery allows a client to advertise its service without a centralized server. After connecting to the access point, the BDE-WF3135N device provides critical information, such as device name, IP, vendor, and port number.
- DHCP server
- Ping

Table 5-1 summarizes the NWP features.

Table 5-1. NWP Features

Feature	Description
Wi-Fi standards	802.11a/b/g/n station 802.11a/b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi channels	2.4 GHz ISM and 5 GHz U-NII Channels
Channel Bandwidth	20 MHz
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal(1)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 with DAD
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW

Table 5-1. NWP Features (continued)

Feature	Description
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key
Power management	Enhanced power policy management uses 802.11 power save and deep-sleep power modes
Other	Transceiver Programmable RX filters with event-trigger mechanism Rx Metrics for tracking the surrounding RF environment

(1) Supported from Service Pack v4.5.0.11-3.1.0.5-3.1.0.25. Limited to STA mode only.

5.2.2.1Security

The BDE-WF3135N internet-on-a chip module enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet security

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP

- **Enterprise standards**
  - EAP Fast
  - EAP PEAPv0 MSCHAPv2
  - EAP PEAPv0 TLS
  - EAP PEAPv1 TLS EAP LS
  - EAP TTLS TLS
  - EAP TTLS MSCHAPv2
- **Secure sockets**
  - Protocol versions: SSL v3/TLS 1.0/TLS 1.1/TLS 1.2
  - On-chip powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256

    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- The trusted root-certificate catalog verifies that the CA used by the application is trusted and known secure content delivery.
- The TI root-of-trust public key is a hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys.
- Secure content delivery allows file transfer to the system in a secure way on any unsecured tunnel.

- Code and data security
  - Secured network information: Network passwords and certificates are encrypted
  - Secured and authenticated service pack: SP is signed based on TI certificate

5.3 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by pulling or forcing SOP[2:0] = 011 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial Flash vendor.

5.4 Hostless Mode

The BDE-WF3135N device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet

- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

Note

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
- The scripter is limited to 16 pairs of conditions and reactions.
- Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
- Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.

---

6. Mechanical Specifications

6.1 Dimensions

The module dimensions are presented in the following figure 14(mm):

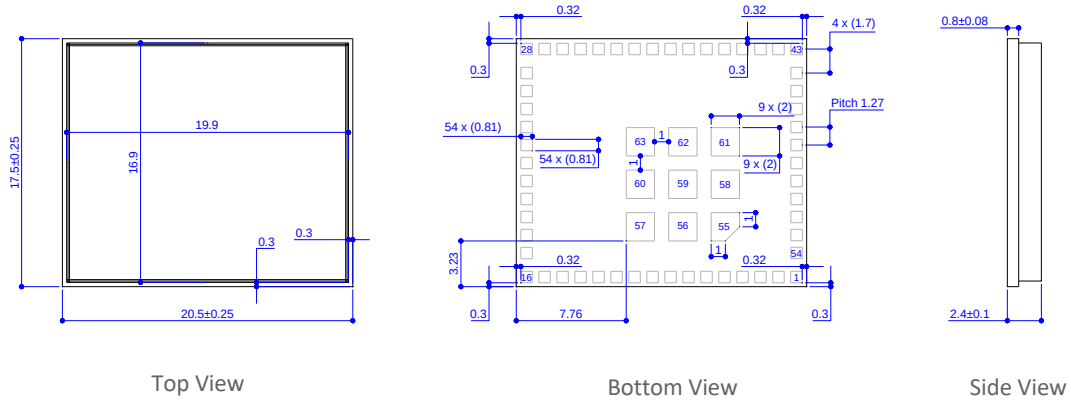

Figure 14. Mechanical Drawing

7. Application Information

7.1 BLE/2.4 GHz Radio Coexistence

The BDE-WF3135N device is designed to support BLE/2.4 GHz radio coexistence. Because WLAN is inherently more tolerant to time-domain disturbances, the coexistence mechanism gives priority to the Bluetooth® low energy entity over the WLAN. Bluetooth® low energy operates in the 2.4 GHz band, therefore the coexistence mechanism does not affect the 5 GHz band. The BDE-WF3135N device can operate normally on the 5 GHz band, while the Bluetooth® low energy works on the 2.4 GHz band without mutual interference.

The following coexistence modes can be configured by the user:

- Off mode or intrinsic mode
  - No BLE/2.4 GHz radio coexistence, or no synchronization between WLAN and Bluetooth® low energy—in case Bluetooth® low energy exists in this mode, collisions can randomly occur.
- Time Division Multiplexing (TDM, Dual Antenna)
  - Dual-band Wi-Fi (see Figure 16)

    In this mode, the WLAN can operate on either a 2.4 or 5 GHz band and Bluetooth® low energy operates on the 2.4 GHz band.

Figure 16 shows the dual antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5 GHz band. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the BDE-WF3135N device is required.

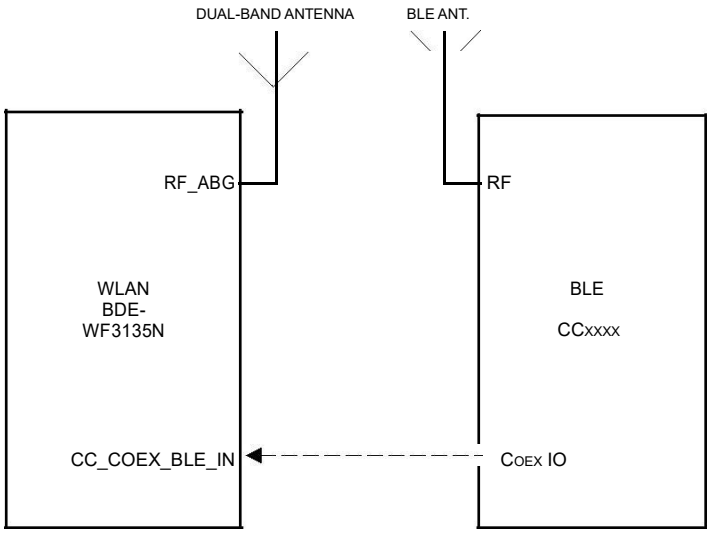

Figure 16. Dual-Antenna Coexistence Mode Block Diagram

7.2 Antenna Selection

The BDE-WF3135N device is designed to also support antenna selection and is controlled from Image Creator. When enabled, there are 3 options possible options:

- ANT 1: When selected, the GPIOs that are defined for antenna selection with set the RF path for antenna 1.
- ANT 2: When selected, the GPIOs that are defined for antenna selection will set the RF path for antenna 2.
- Auto select: When selected, during a scan and prior to connecting to an AP, BDE-WF3135N device will determine the best RF path and select the appropriate antenna. The result is the saved as port of the profile.

Figure 17 shows the antenna selection implementation for Wi-Fi, with BLE operating on it's own antenna. Note in this implementation, only a single GPIO from the BLE device to the BDE-WF3135N device is required. The Antenna switch is controlled by 2 GPIO lines from the BDE-WF3135N device.

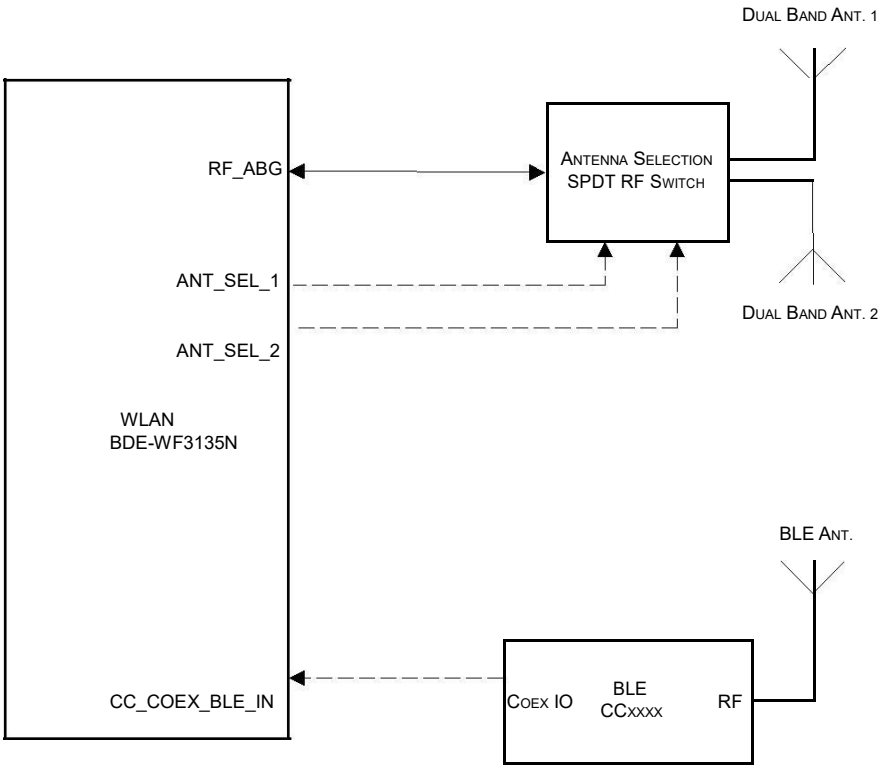

Figure 17. Coexistence Solution with Wi-Fi Antenna Selection and dedicated BLE antenna

7.3 Typical Application

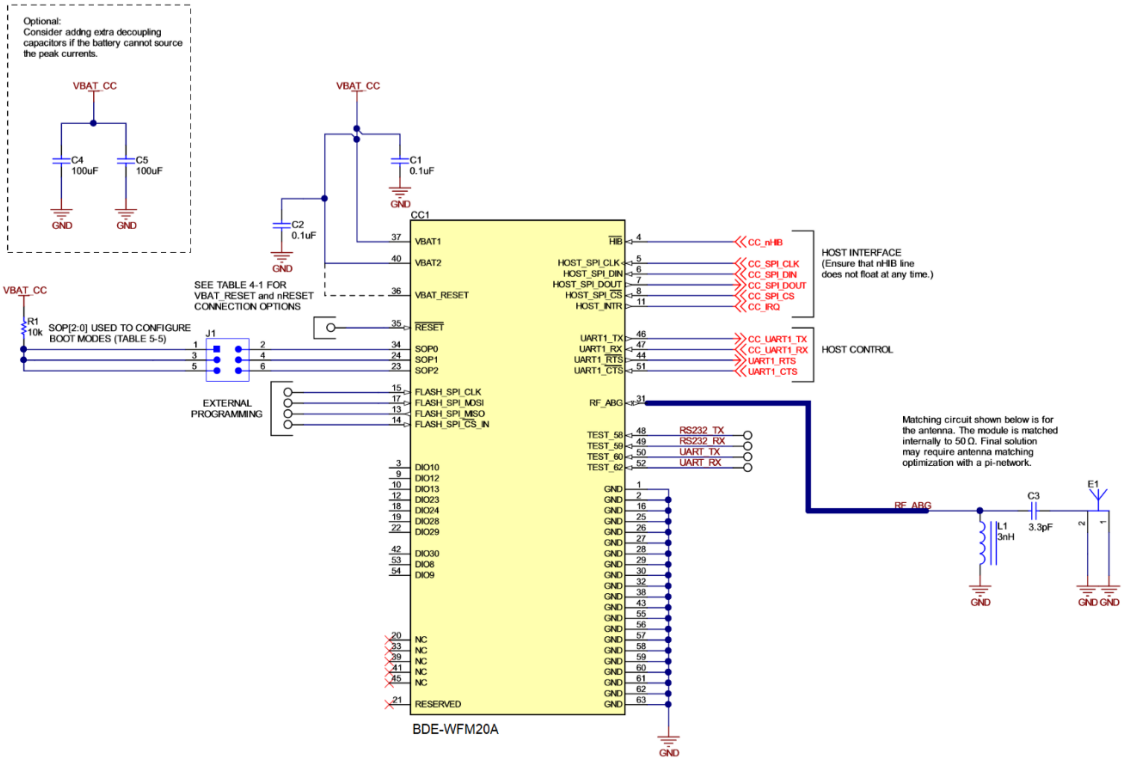

Figure 18. BDE-WF3135N Module Reference Schematic

Note

The following guidelines are recommended for implementation of the RF design:

- Ensure an RF path is designed with an impedance of 50 Ω
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics
- π or L matching and tuning may be required between cascaded passive components on the RF path

Table 7-1. Bill of Materials

QTY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
2	C1, C2	0.1 uF	Murata	GRM155R61A104KA01D	Capacitor, ceramic, 0.1 uF, 10 V, ±10%, X5R, 0402
1	C3	3.3 pF	Murata	GJM1555C1H3R3BB01	Capacitor, ceramic, 3.3 pF, 50 V, ±0.1pF, C0G/NP0,0402
2	C4, C5	100 uF	Murata	LMK325ABJ107MMHT	Capacitor, ceramic, 100 uF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
1	E1	2.4 GHz, 5 GHz Ant	Ethertronics	M830520	Antenna Bluetooth WLAN Zigbee®
1	L1	3 nH	Murata	LQG15HS3N0S02D	Inductor, Unshielded, Multilayer, 3nH, 0.8 A, 0.125Ω, SMD
1	R1	10k	Vishay-Dale	CRCW040210K0JNED	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402
1	CC1	BDE-WF3135N	Texas Instruments	CC3135MODRNMMOBR	Wi-Fi® Dual-Band Network Processor Internet-of-Things Module Solution for MCU Applications, MOB0063A

7.4 Power Supply Decoupling and Bulk Capacitors

Depending upon routing resistors and battery type, TI recommends adding two 100-µF ceramic capacitors to help provide the peak current drawn by the BDE-WF3135N module.

7.5 Reset

The module features an internal RC circuit to reset the device during power ON. The nRESET pin must be held below 0.6 V for at least 5 ms for the device to successfully reset.

7.6 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current.

8. Ordering Information

Table 10-1: Ordering Information

Part Number	Size (mm)	Shipping Form	MOQ
BDE-WF3135N	20.5 x 17.5 x 2.4	Tape & Reel	1000

9. Regulatory Information

To be defined

Revision History

Revision	Date	Description
V1.0	27- Dec -2020	Initial Released
V2.0	27- Dec -2021	Change Moudle's name
V2.1	30- Aug -2023	Picture, Size

Contacts

BDE Technology Inc.

USA: 67 E Madison St, # 1603A, Chicago, IL 60603, US
Tel: +1-312-379-9589
Website: http://www.bdecomm.com Email: info@bdecomm.com

China: B2-403, 162 Science Avenue, Huangpu District, Guangzhou 510663, China
Tel: +86-20-28065335
Website: http://www.bdecomm.com Email: sales@bdecomm.comm