General Description

BDE-HWF7394N is an ultra-low power & long-range Wi-Fi module based on IEEE 802.11ah, a new Wi-Fi standard operating in the Sub 1GHz license-exempt band, offering longer range and lower power connectivity necessary for internet of things (IoT) applications.

The module can operate at frequency range from 740 MHz to 950 MHz for different countries/regions. Refer to Table 1 for different variants targeting at different counties.

With the internal PA in SoC, the module can increase transmission power up to 16 dBm. It outputs the accurate power for each channel through the temperature sensor integrated in the SoC and calibration at the factory. On-board serial flash can be used for user application program and OTA software update and store MAC address, calibration data and information. It also can support execution in place (XIP) feature with a 16KB internal cache memory.

Table 1. Module Variants

Orderable Part Number	Country/Region
BDE-HWF7394N-915	US, Japan, Korea, Singapore
BDE-HWF7394N-865	Europe
BDE-HWF7394N-750	China

Key Features

- **Standard**
  - Full IEEE 802.11ah compatibility with enhanced performance
  - 1/2/4 MHz channel bandwidth, up to 15Mbps data rate
  - WPA2/WPA3/WPS support
  - Support transmission of standby radio frame
- **Radio Frequency**
  - +16 dBm transmit power
  - -106 dBm minimum receive sensitivity (MCS10)
  - 740~950 MHz frequency band by different module variants
- **Main Interface**
  - UART and SPI support for host interface
- **Peripherals**
  - GPIO, AUXADC
  - I2C, SPI and UART
- **RF Transceiver**
  - Based on the industry-proven direct conversion transceiver architecture
  - Includes a complete radio front-end part, which consists of a TX power amplifier and an LNA
  - Integrated LDOs
  - Wide supply voltage supportable with an

integrated DC-DC buck converter
- Usable battery voltage range: 2.1V ~ 3.6V
- Radio calibration interfaces for digital baseband
- Internal temperature sensing and battery voltage monitoring
- Low supply current:
  - RX 15 mA @ 3.3V
  - TX 190 mA @ 3.3V @ +15 dBm
- Modulation bandwidth: 1/2/4 MHz
- RX noise figure < 6dB
- RX gain range: > 100dB
- RX IIP3: -17dBm @ LNA maximum gain
- Linear output power: +15 dBm
- TX gain range: > 30 dB
- EVM < -30 dB @ +15 dBm (w/ 64 QAM, DPD)
- Integrated RF PLL phase error < 0.7 degree

■ **BUS Sub-System**
- Firmware code can be stored and executed in external flash memory using XIP (execute-in-place) interface
- System Peripherals
  - 3 channel 32-bit timers
  - 1 channel 64-bit timers
  - 1 channel 32-bit watchdog timers
  - 1 channel 64-bit RTC with offset estimator
  - Serial flash controller for XIP with cache (16KB cache memory)
- General Direct Memory Controller
  - 8 DMA channels with 2 AHB masters
  - 16 controls for communicating with peripherals
- Data Peripherals
  - Max 20 general purpose I/Os
  - 1 HSPI(Host SPI) for host interface
  - 2 channel SPIs master/slave
  - 2 channel HSUARTs, up to 115200 baud rate
  - 2 channel I2C masters
  - 4 channel PWM generator
  - 10-bit ADC: 2ch input

■ **MAC**
- Basic features: S1G Beacon, NDP Control frame, TIM compression, unified scaling factor for max idle period/listen interval/WNM-sleep interval, STA Type, S1G baseline functions (DCF, HCF, multi-rate support, A-MPDU), and S1G BSS operation
- Network efficiency enhancements: NDP PS-Poll/PS-Poll Ack/Probe Resp., Raw avoidance, TSBTT, and differentiated EDCA parameter
- Power saving: Non-TIM operation, dynamic AID assignment and TWT
- BSS scalability (up to 8192 STAs): Multicast AID, and authentication control
- Low-cost STA/AP: EL operation, flow control
- Supports transmission of Standby Radio frame

■ **PHY**
- Full IEEE 802.11ah compatibility with enhanced performance
- Single-stream up to 15Mbps data rate
- Support 1/2/4 MHz channel with optional SGI
- Support S1G_1M, Short/Long format
- Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM

■ **Memory**
- 32KB Boot ROM
- 1088KB system SRAM
  - SRAM0: 512KB
  - SRAM1: 320KB
  - SRAM2: 192KB
  - SRAM3: 16KB
  - SRAM4: 48KB (Retention)
- 192KB Key memory for security
  - This memory could be used as additional 192KB SRAM2 in non-key memory & boot mode
- 16KB cache for XIP
  - This memory could be used as additional 16KB SRAM3 in non-cache & boot mode
- On-board 4Mbyte serial flash for XIP

- **Antenna**
  - ANT pin for external antenna
- **Regulatory**
  - FCC
  - IC
  - CE
- **Package**
  - Dimension: 13.5 mm x 13.5 mm x 2.1 mm

Applications

- Smart home and home security
- Smart factory and factory automation
- Smart city and public transportation management
- Smart grid/metering
- Surveillance camera and remote monitoring
- Wireless sensor network
- Health care
- Electric vehicle and charging
- Commercial drone

Reference

[1] NRC7394 resources: https://newracom.com/products/nrc7394

Contents

List of Tables

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1. System Overview

1.1. Block Diagram

BDE-HWF7394N is based on Newracom's next generation Wi-Fi Halow SoC NRC7394.

The block diagram of the module can be seen in Figure 1, comprises of:

- 32-MHz HFXT
- 32.768-KHz LFXT
- Power inductors and capacitors
- 32-Mbit SPI flash
- SPDT RF switch
- SAW filter
- Discrete low pass filter

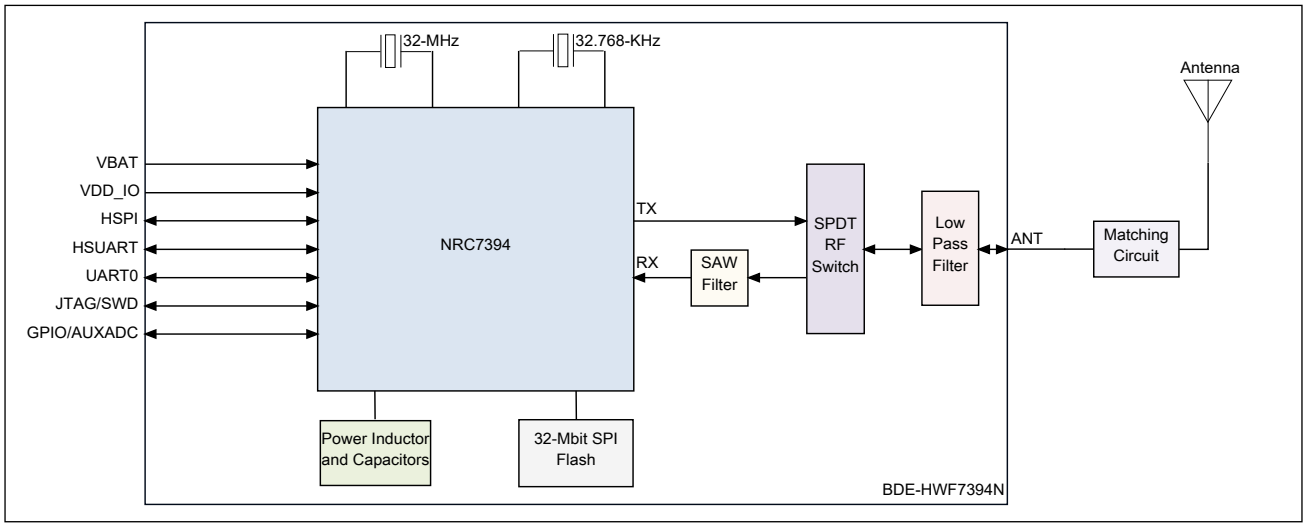


Figure 1. The Block Diagram of BDE-HWF7394N

1.2. ARM® Cortex®-M3 CPU

The module is based on Newracom's NCR7394 SoC which has an ARM® Cortex®-M3 processor and a single AHB BUS subsystem that can accommodate the 802.11ah modem and various peripherals on a single die.

The Cortex®-M3 processor is a low-power RISC processor that features low gate count, low interrupt latency, and low-cost debug. It is for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M.

This processor is used to implements the higher layers of IEEE802.11ah (HaLow) protocol as well as a simple user

application program like a sensor application.

1.3. Power Management System

PMS is a subsystem that creates the required power in SoC NRC7394. It consists of a highly efficient DC-DC BUCK converter and several LDOs. Therefore, a single DC power range from 2.4 to 3.6V is sufficient to drive the NRC7394 without any additional voltage regulator.

The module has two inputs: VBAT and VDD_IO. The voltage level of external IOs can be set by VDD_IO. This offers user flexibility in designing system interfaces. VDD_IO can be connected to VBAT if the 3.3V voltage level is selected.

1.4. Clock

The module has two crystal oscillators with frequencies 32 MHz and 32.768 kHz. 32 MHz oscillator is the main clock source for CPU, BUS, RF, and modem circuits. 32.768 kHz clock is mainly used for Real Time Clock (RTC) and Power Save (PS) mode operation to reduce power consumption.

1.5. Boot Mode

MODE pin is provided for boot mode selection to offer flexible and configurable boot options as shown in following table. In the case of XIP boot, it is necessary to change to XIP boot mode after FW upload, so users need to install a switch that can control the mode pins on the board.

Table 2. MODE Pin Description

MODE Pin Input Level	Description
High/VDD_IO	XIP boot mode F/W should be downloaded in external flash memory before power on. The start address for boot is remapped to the start address of flash memory.
Low/GND	Boot ROM mode Boot from in ternal ROM code and wait for external command via HSPI or UART. The start address for boot is remapped to the start address of ROM memory.
	FW upload mode Firmware upgrade to external flash memory or upload to internal SRAM via UART0.

1.6. Memory

The module includes the following memories.

- ROM for boot of Cortex®-M3
- SRAM for internal memory
- SRAM4 for retention memory

- 192KB of key memory for security from MAC
- 16KB of cache memory for XIP from external flash memory

SoC NRC7394 memory map can be configured by boot mode or user setting. Default boot region (0x00000000) is mapped with physical memory and it depends on MODE pin configuration during reset sequence.

The module has an on-board 32-Mbit external serial flash memory for storing RF calibration data, MAC addresses, and programs.

1.7. E-FUSE

SoC NRC7394 has an internal 1024-bit one-time programmable electrical fuse (E-FUSE). It is used to store device-specific configuration information like PMS and RF calibration parameters and so on.

2. Pinout Functions

The module is with LGA-32 package, 32 pads are exposed for user. This section describes pinout functions of the module in details.

2.1. Pinout Diagram

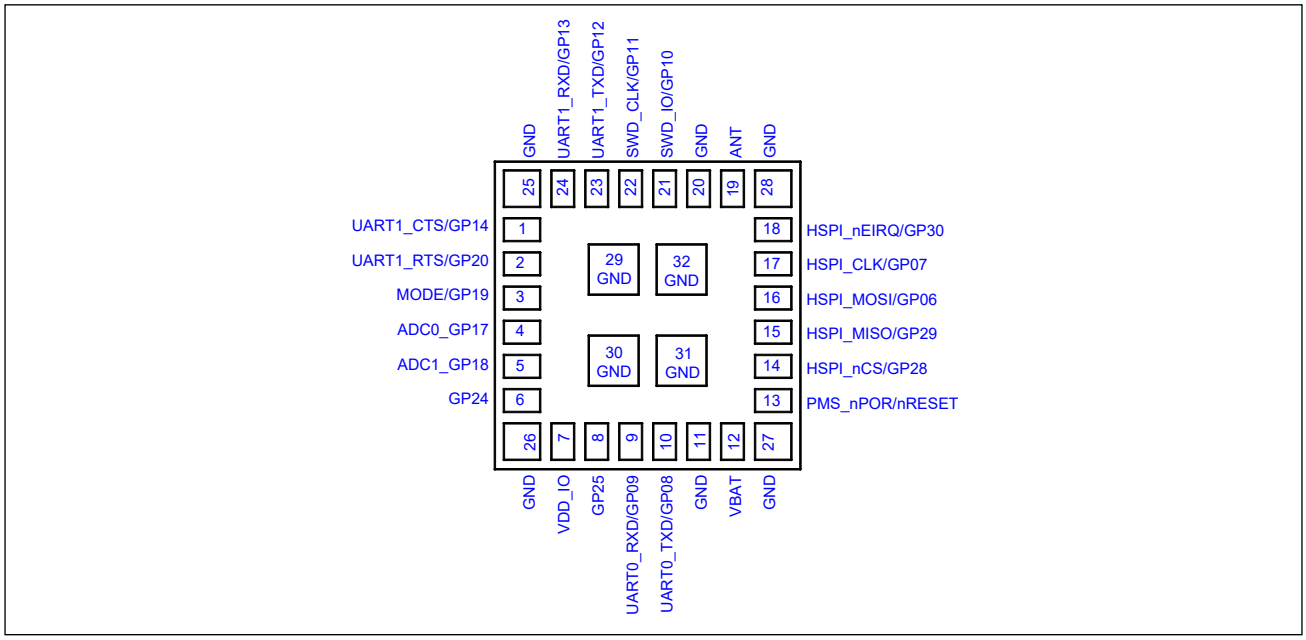


Figure 2. Pinout Diagram of BDE-HWF7394N Top View

The following I/O pins of the SoC are assigned to the on-board 32-Mbit SPI flash:

- GP5 as XIP_nCS
- GP4 as XIP_nHOLD
- GP3 as XIP_nWP
- GP2 as XIP_MISO
- GP1 as XIP_MOSI
- GP0 as XIP_CLK

2.2. Pinout Descriptions

Table 4 describes the definitions of the pins of the module. Pin number of NRC7394 chip is also stated.

Table 3. Pinout Description

Module Pin #	Pin Name	Direction	NRC7394 Pin #	Description
1	UART1_CTS/GP14	I	5	UART channel 1 clear to send; GPIO 14.
2	UART1_RTS/GP20	O	7	UART1 channel 1 request to send; GPIO 20.
3	MODE/GP19	I	8	Boot mode (0: ROM boot, 1: XIP boot), **refer to Section 1.6;** GPIO 19.
4	ADC0/GP17	I	18	Auxiliary ADC channel 0; GPIO 17.
5	ADC1/GP18	I	19	Auxiliary ADC channel 1; GPIO18.
6	GP24	I/O	22	GPIO **24**
7	VDD_IO	P	6, 24	I/O power input
8	GP25	I/O	23	GPIO **25**
9	UART0_RXD/GP09	I	46	UART channel 0 R**X** data; GPIO 09.
10	UART0_TXD/GP08	O	45	UART channel 0 T**X** data; GPIO 08.
11	GND	GND	-	Ground
12	VBAT	P	9, 10, 36	**Main power,** PMS, RF/PA power input
13	PMS_nPOR/nRST	I/O	40	**R**eset (active low) input; POR reset output (internal pull-up)**.**
14	HSPI_nCS/GP28	I	41	Host SPI – chip select (active low); GPIO 28.
15	HSPI_MISO/GP29	O	42	Host SPI – master in slave out; GPIO 29.
16	HSPI_MOSI/GP06	I	43	Host SPI – master out slave in; GPIO 06.
17	HSPI_CLK/GP07	I	44	Host SPI **–** clock; GOIO 07.
18	HSPI_nEIRQ/GP30	O	47	Host SPI – interrupt (active low); GPIO 30.
19	ANT	I/O	-	Antenna port
20	GND	GND	-	Ground

Module Pin #	Pin Name	Direction	NRC7394 Pin #	Description
21	SWD_IO/GP10	I/O	48	SWD data; GPIO 10.
22	SWD_CLK/GP11	I	2	SWD clock; GPIO 11.
23	UART1_TXD/GP12	O	3	UART channel 1 T**X** data; GPIO 12.
24	UART1_RXD/GP13	I	4	UART channel 1 R**X** data; GPIO 13.
25	GND	GND	-	Ground
26	GND	GND	-	Ground
27	GND	GND	-	Ground
28	GND	GND	-	Ground
29	GND	GND	-	Ground, thermal pad
30	GND	GND	-	Ground, thermal pad
31	GND	GND	-	Ground, thermal pad
32	GND	GND	-	Ground, thermal pad

2.3. Connections for Unused Pins

Table 4. Connections for Unused Pins

Function	Signal Name	Acceptable Practice	Proffered Practice
GPIO (Digital or analog)	GPn	NC, GND or VDD	NC
SWD	SWD_IO, SWD_CLK	NC, GND or VDD	NC

2.4. GPIO Multiplexed Functions

Table 5 presents the multiplexed function of IO pins.

Table 5. GPIO Multiplexed Functions

Module Pin #	Pin Name	Pin description	ALT Function Definition			
			ALT0	ALT1	ALT2	ALT3
16	GP6	General Port IO 6	GBUS	WAKEUP0	HSPI_MOSI	
17	GP7	General Port IO 7	GBUS	WAKEUP1	HSPI_CLK	
10	GP8	General Port IO 8	GBUS	WAKEUP0	-	
9	GP9	General Port IO 9	GBUS	WAKEUP1	-	
21	GP10	General Port IO 10	GBUS	WAKEUP0	TMS/SWDIO	
22	GP11	General Port IO 11	GBUS	WAKEUP1	TCL/SWDCLK	
23	GP12	General Port IO 12	GBUS	WAKEUP0	TDO	
24	GP13	General Port IO 13	GBUS	WAKEUP1	TDI	

Module Pin #	Pin Name	Pin description	ALT Function Definition			
			ALT0	ALT1	ALT2	ALT3
1	GP14	General Port IO 14	GBUS	WAKEUP0	nTRST	TOUT0
4	GP17	General Port IO 17	GBUS	WAKEUP0	AUXADC0	TOUT3
5	GP18	General Port IO 18	GBUS	WAKEUP0	AUXADC1	
3	GP19	General Port IO 19	GBUS	WAKEUP1	MODE	
2	GP20	General Port IO 20	GBUS	WAKEUP0	-	
6	GP24	General Port IO 24	GBUS	WAKEUP0	PA_EN	
8	GP25	General Port IO 25	GBUS	WAKEUP1	-	
14	GP28	General Port IO 28	GBUS	WAKEUP0	HSPI_CS	
15	GP29	General Port IO 29	GBUS	WAKEUP1	HSPI_MISO	
18	GP30	General Port IO 30	GBUS	WAKEUP0	HSPI_EIRQ	

When configured as an output, GPIO pins can function as push-pull. If the S/W controls output direction with holding 0 in output data register, GPIO pins can function as open-drain.

3. Characteristics

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Over operating free-air temperature range (unless otherwise noted).

Table 6. Absolute Maximum Ratings

Parameter		Min	Max	Unit
Storage temperature range (T_{STG})		-40	+125	°C
Supply voltage	VBAT	-0.5	3.8	V
	VDD_IO	-0.5	3.8	V
	Analog/ANT pin	-0.5	2.1	V

3.1.2. ESD Ratings

Table 7. ESD Ratings

Parameter	Description	Value	Unit	Note
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

3.1.3. Recommended Operating Conditions

Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.

Over operating free-air temperature range (unless otherwise noted).

Table 8. Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
Operating temperature range		-40	-	+85	°C
Operating voltage	VBAT	2.4	3.3	3.6	V
	VDD_IO	1.68	3.3	3.6	V
Peak operating current TX @16dBm	VBAT	250			mA
	VDD_IO	2			mA

Note:

(1) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300mV.

3.1.4. Power Consumption

Condition: VBAT = 3.3V. Power as ICC*VBAT, ICC measured as current into VBAT terminal.

Table 9. Power Consumption

Mode	Min	TYP	Max	Unit	Comments
Deep sleep		3.5		μA	RTC on 48KB retention memory
Receive		21		mA	Decode received signal and ready to response
Transmit (+15dBm out)		180		mA	Transmit 2 MHz BW signal with internal PA
Transmit (+17dBm out)		195		mA	Transmit 2 MHz BW signal with internal PA

Table 10. Current Consumption (Average)

MODE	DUT Status	VDD_IO (mA)	VBAT (mA)
802.11ah (1/2/4MHz BW)	TX @ 0 dBm	1.45	105.2
	TX @ 10 dBm	1.48	169.2
	TX @ 15 dBm	1.53	184.4
	Continuous Rx @ -85 dBm	1.44	20.7
	Deep sleep mode	0.08uA	3.2uA

Note:

(1) Unless otherwise specified, TA.=25°C, VBAT=3.3V, 99% TX burst time, MCS0, 915MHz;
(2) Deep sleep: all clocks are gated, 32M & 32K XTALs off, all power off(except ALON), retention memory off;

(3) HSPI pins to host are disconnected.

3.1.5. Clock Characteristics

The characteristics of the two XTALs included in the module are listed in below tables.

Table 11. 32-MHz Crystal Oscillator (HFXT) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32		MHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-10		+10	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			7		pF

Table 12. 32.768-KHz Crystal Oscillator (LFXT) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32.768		KHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-20		+20	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			12.5		pF

3.1.6. Power on Sequence

The start of the POR circuits in the PMS block and BUCK oscillator in SoC are triggered by VABT when the level exceeds a predefined voltage level. The main 32M crystal starts to run when the internal power supply is stable.

VDD_IO must be supplied simultaneously with VBATT or within 10msec after VBATT is supplied and before PMS_nPoR goes high.

In general, it is recommended to supply VABTT and VDD_IO sequentially, or to supply 2 powers simultaneously.

When the PMS_nPoR release the pin to HIGH, the power-on sequence is completed and the SoC cancontrol the entire system after the internal 25usec reset time.

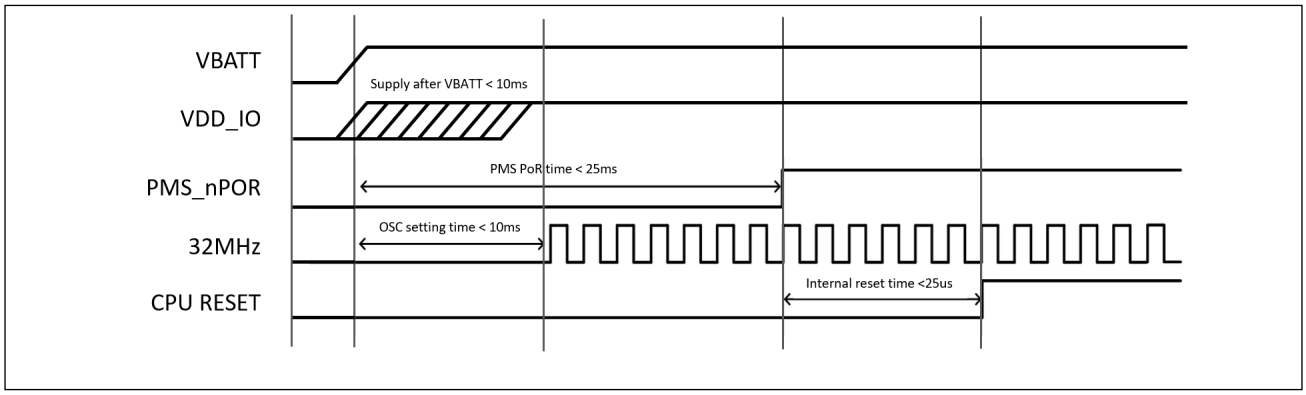


Figure 3. Power-On Sequence

3.1.7. HSPI timing

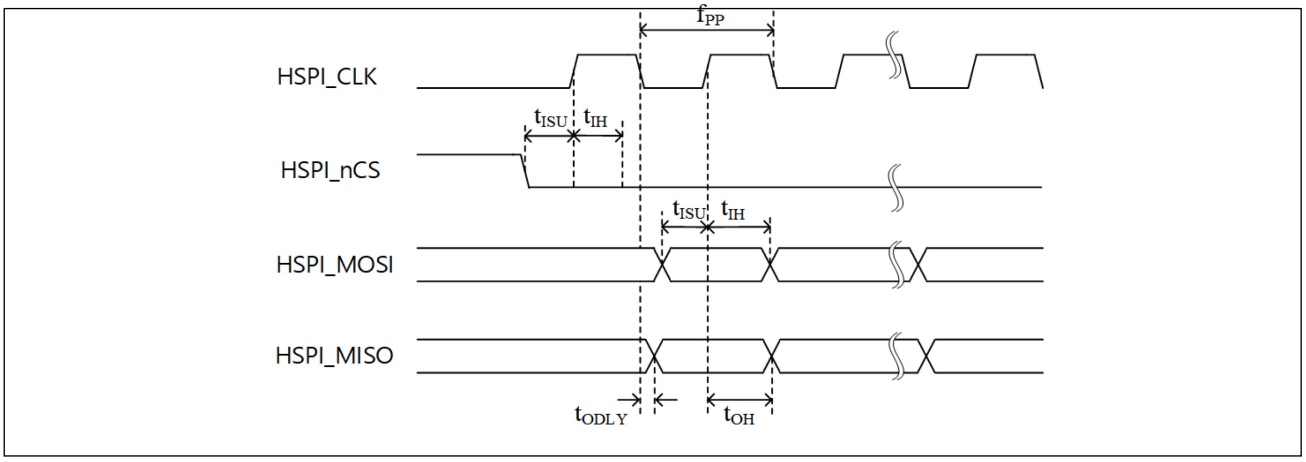


Figure 4. Timing Diagram of HSPI

Table 13. HSPI timing data

Symbol	Parameter	MIN	TYP	MAX	Unit
f_{PP}	Frequency	-	-	20	MHz
t_{ODLY}	Output delay time	2.7	-	20.2	ns
t_{OH}	Output hold time	25	-	-	ns
t_{ISU}	Input setup time	-	-	21.6	ns
t_{IH}	Input hold time	5.8	-	-	ns

3.1.8. SPI timing

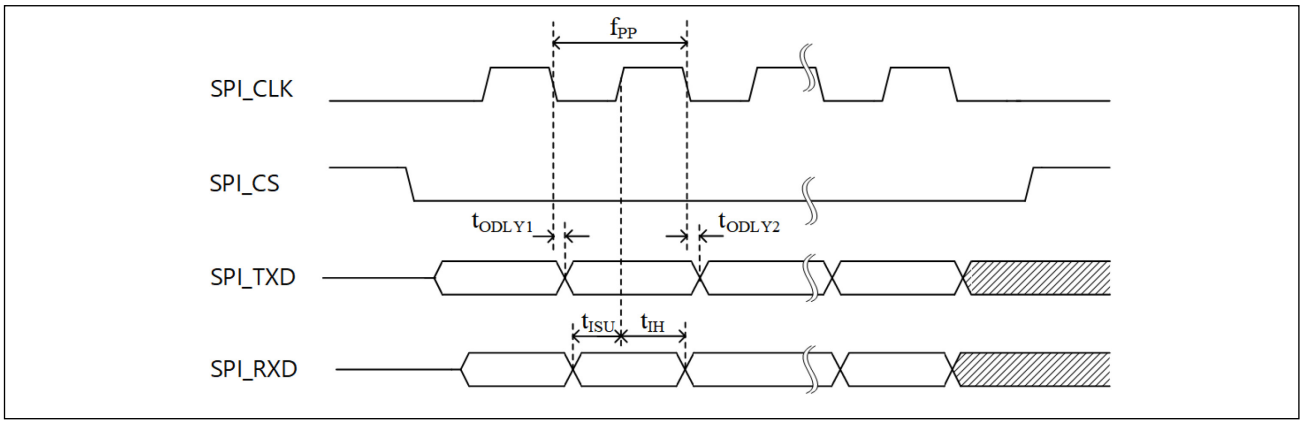


Figure 5. Timing Diagram of SPI

Table 14. SPI Timing Data

Symbol	Parameter		MIN	TYP	MAX	Unit
f_{PP}	Frequency	master	-	-	16	MHz
		slave	-	-	2	MHz
t_{ODLY1}	Output delay time1		0	-	23	ns
t_{ODLY2}	Output delay time2		0	-	23	ns
t_{ISU}	Input setup time		18	-	-	ns
t_{IH}	Input hold time		20	-	-	ns

3.1.9. XIP(eXecute In Place) Timing

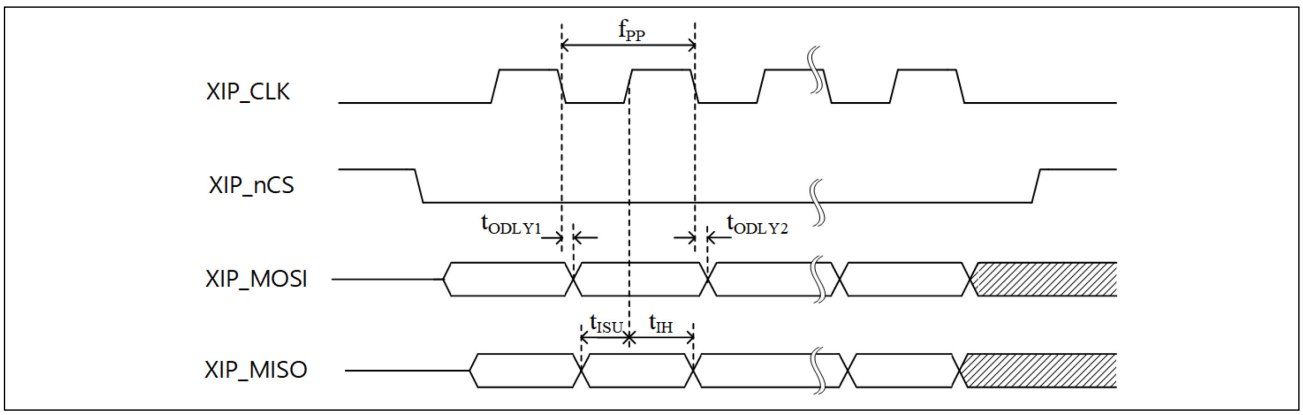


Figure 6. Timing Diagram of XIP

Table 15. XIP Timing Data

Symbol	Parameter	MIN	TYP	MAX	Unit

f_{PP}	Frequency	-	-	32	MHz
t_{ODLY}	Output delay time1	0	-	15	ns
t_{ODLY2}	Output delay time2	0	-	15	ns
t_{ISU}	Input setup time	-	-	5.1	ns
t_{IH}	Input hold time	7.7	-	-	ns

3.1.10. I2C Timing

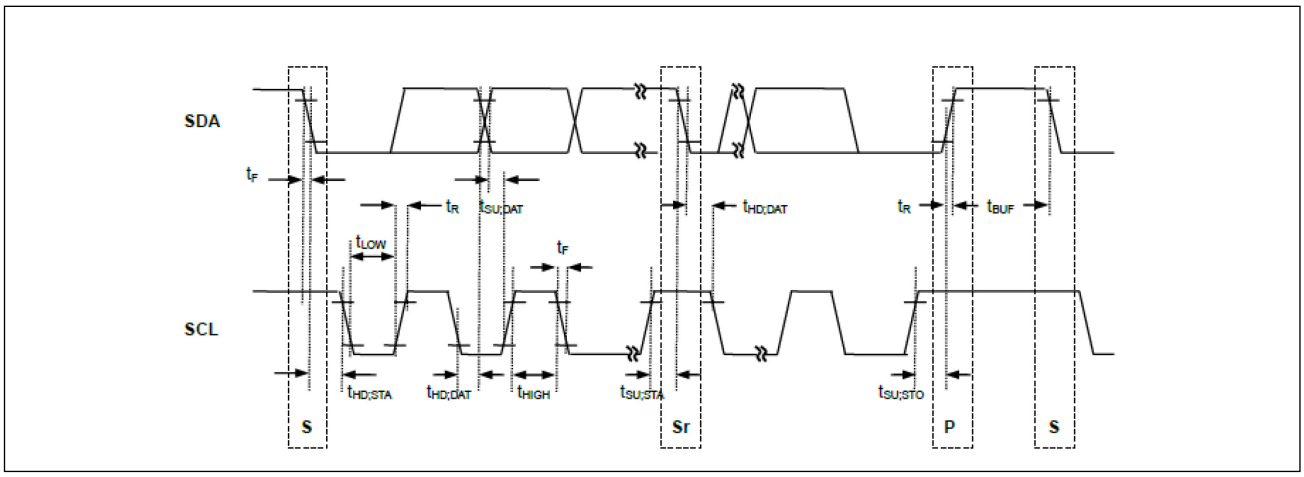


Figure 7. Timing Diagram of I2C

Table 16. I2C Timing Data

Symbol	Parameter	STANDARD MODE		FAST MODE		
		Min	Max	Min	Max	Unit
f_{SCL}	SCL frequency	0	100	0	400	KHz
$T_{HD;STA}$	Hold time after START condition	4.0	-	0.6	-	us
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	High period of the SCL clock	4.0	-	0.6	-	us
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	-	0.6	-	us
$t_{HD;DATA}$	Data hold time	0	3.45	0	0.9	us
$t_{SU;DATA}$	Data setup time	100	-	100	-	us
t_F	Clock/data fall time	0	300	0	300	us
t_R	Clock/data rise time	0	1000	0	1000	us
$t_{SU;STO}$	Setup time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	us

3.1.11. AUXADC Timing

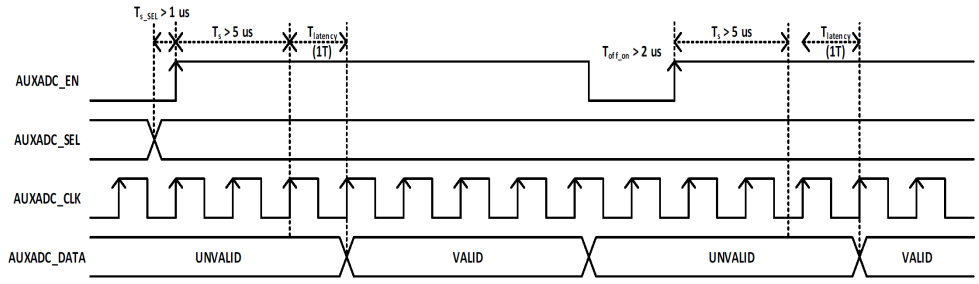


Figure 8. Timing Diagram of AUXADC

Table 17. AUXADC Timing Data

Symbol	Parameter	MIN	TYP	MAX	Unit
Input Range	Input signal range	0.1		0.9	V
Output Range	Output Code Range (After s/w compensation)	100		900	10-bit
FS	Sampling clock	-	2	-	MHz
Latency	Conversion latency (1 cycle = T)	-	1	-	cycle
N	Resolution	-	10	-	Bit
RIN	Input impedance	-	4	-	Mohms
Ts	Settling time after enable	5			us
Ts_sel	Setup time of AUXADC_SEL	1			us
Toff_on	Reset time	2			us
I_active	Current consumption (1.1V)	-	-	150	uA
I_down	Power-down current (1.1V)	-	-	2	uA

3.2. 802.11ah WLAN RF Specification and Performance

3.2.1. Transmitter Characteristics

Table 18. Transmitter Characteristics

Parameter	Condition	Min	Typ	Max	Unit
RF output frequency range (1)		902		928	MHz
EVM complaint output power	MCS7, 4MHz BW, VBAT=3.3V		13		dBm
EVM at 0 dBm output power			-32.5		dB
Transmitter spurious signal emissions	< 700 MHz		<-36		dBm/ MHz
	> 1GHz		<-45		

Note:

(1) Only 902 to 928MHz frequency range data is recoded.

3.2.2. Transmitter EVM

Table 19. Tx power and EVM

Band	BW	MCS	Modulation / Coding Rate	EVM Spec [dB]	MAX. Power [dBm]
902 ~ 928 MHz (1)	1 MHz	10	BPSK 1/2 rep. 2x	-4	16
		0	BPSK 1/2	-5	16
		1	QPSK 1/2	-10	16
		2	QPSK 3/4	-13	16
		3	16QAM 1/2	-16	16
		4	16QAM 3/4	-19	15
		5	64QAM 2/3	-22	14
		6	64QAM 3/4	-25	13
		7	64QAM 5/6	-27	12
	2 MHz	0	BPSK 1/2	-5	16
		1	BPSK 3/4	-10	16
		2	QPSK 1/2	-13	16
		3	QPSK 3/4	-16	16
		4	16QAM 1/2	-19	15
		5	16QAM 3/4	-22	14
		6	64QAM 2/3	-25	13
		7	64QAM 3/4	-27	12
	4 MHz	0	BPSK 1/2	-5	16
		1	QPSK 1/2	-10	16
		2	QPSK 3/4	-13	16
		3	16QAM 1/2	-16	16
		4	16QAM 3/4	-19	15
		5	64QAM 2/3	-22	14
		6	64QAM 3/4	-25	13
		7	64QAM 5/6	-27	12

Note:

(1) Only 902 to 928MHz frequency range data is recoded.

3.2.3. Receiver Characteristics

Table 20. Receiver Charcteristics

Parameter	Condition	Min	Typ	Max	Unit
RF input frequency range (1)		902		928	MHz
RF input return loss	For LNA high/mid/low gain modes	-10	-12	-15	dB
Total voltage gain range	Analog + Digital Gain	-10		92	dB
RF gain step	For high/mid gain mode		7		dB
RX gain step	From RF to Analog		1		dB
DSB noise figure	LNA max gain mode		3.5		dB
IIP3	LNA with high gain mode		-17		dBm
	LNA with low gain mode		24		

Note:

(1) Only 902 to 928MHz frequency range data is recoded.

3.2.4. Receiver Sensitivity

Table 21. Receiver Sensitivity (1)

Band	BW	MCS	Modulation/Coding Rate	11ah Spec [dBm]
902 ~ 928 MHz (2)	1 MHz	10	BPSK 1/2 rep. 2x	-98
		0	BPSK 1/2	-95
		1	QPSK 1/2	-92
		2	QPSK 3/4	-90
		3	16QAM 1/2	-87
		4	16QAM 3/4	-83
		5	64QAM 2/3	-79
		6	64QAM 3/4	-78
		7	64QAM 5/6	-77
	2MHz	0	BPSK 1/2	-92
		1	BPSK 3/4	-89
		2	QPSK 1/2	-87
		3	QPSK 3/4	-84
		4	16QAM 1/2	-80
		5	16QAM 3/4	-76
		6	64QAM 2/3	-75
		7	64QAM 3/4	-74
	4 MHz	0	BPSK 1/2	-89

Band	BW	MCS	Modulation/Coding Rate	11ah Spec [dBm]
		1	QPSK 1/2	-86
		2	QPSK 3/4	-84
		3	16QAM 1/2	-81
		4	16QAM 3/4	-77
		5	64QAM 2/3	-73
		6	64QAM 3/4	-72
		7	64QAM 5/6	-71

Note:

(1) Measured at antenna port @ PER<10%, 256 bytes;
(2) Only 902 to 928MHz frequency range data is recoded.

4. Mechanical Specifications

The following pages include mechanical and footprint drawings of the module.

4.1. Dimensions

The module dimensions are presented in the following figure:

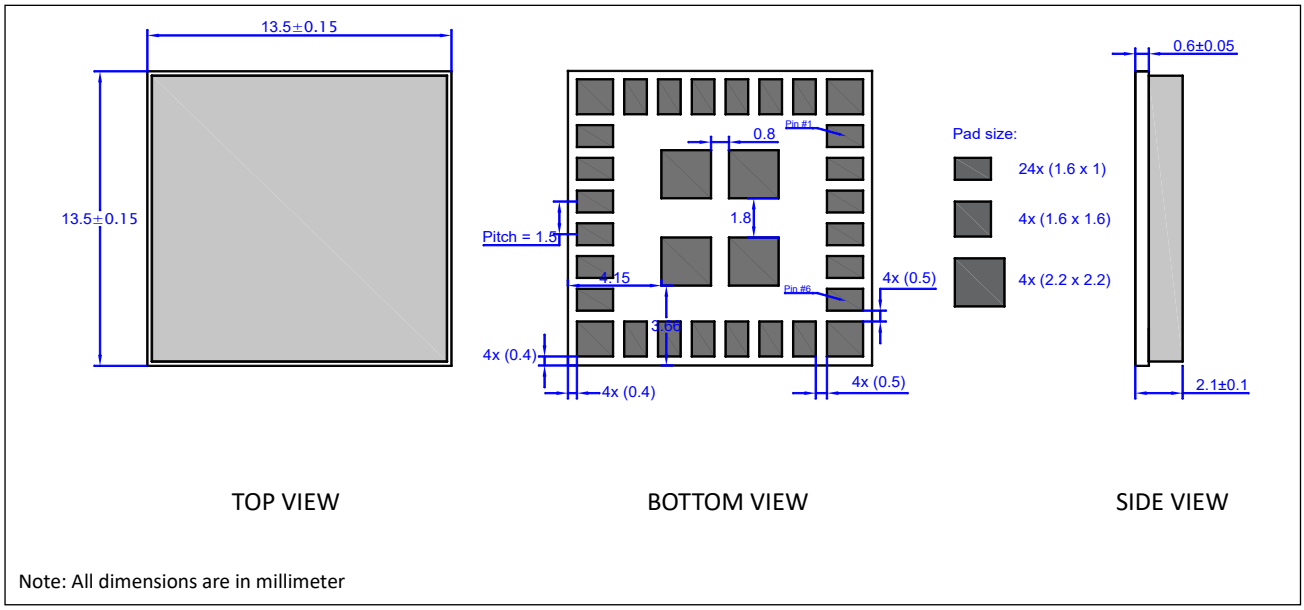
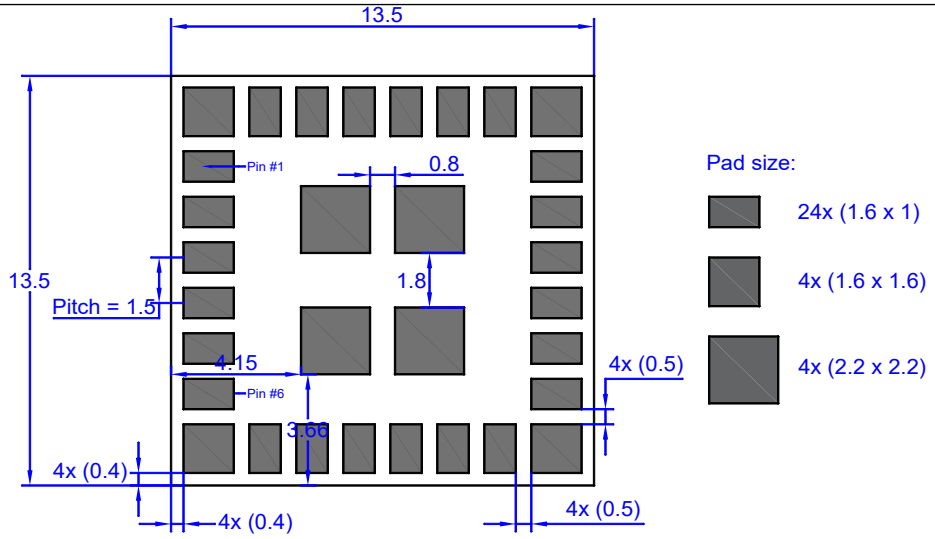


Figure 9. Mechanical Drawing for BDE-HWF7394N

4.2. PCB Footprint

The recommended footprint for the PCB is presented in the following figure:



Note:

(1) All dimensions are in millimeter;
(2) Solder mask should be the same or 5% larger than the dimension of the pad;
(3) Solder paste must be the same as the pin for all peripheral pads. For thermal pads, make the solder paste 20% smaller than the pad;
(4) Copper-free means no copper in this area in all layers, including traces, ground or components ect.
(5) Customers can modify the land pattern dimensions based on their manufacturing experience.

Figure 10. Module Footprint for BDE-HWF7394N Top View

5. Integration Guidelines

TBD

6. Handling Instructions

TBD

7. Certification

TBD

8. Ordering Information

Orderable Part Number	Description	Size (mm)	Package	MOQ
BDE-HWF7394N-915	BDE Ultra-Low Power & Long-Range Wi-Fi Module Based on 802.11ah, 902 MHz to 928 MHz	13.5 x 13.5 x 2.1	Tape & Reel	TBD
BDE-HWF7394N-865	BDE Ultra-Low Power & Long-Range Wi-Fi Module Based on 802.11ah, 863 MHz to 868 MHz	13.5 x 13.5 x 2.1	Tape & Reel	TBD
BDE-HWF7394N-750	BDE Ultra-Low Power & Long-Range Wi-Fi Module Based on 802.11ah, 755 MHz to 787 MHz	13.5 x 13.5 x 2.1	Tape & Reel	TBD

9. Revision History

Revision	Date	Description
V0.1	Jan-30, 2024	Preliminary, draft

You can find the latest documentation with this link.

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