General Description

Note: Images are for illustrative purposes only; actual products may differ.

BDE-BW3551 is a 2.4-GHz & 5-GHz dual-band Wi-Fi 6 and BLE Combo wireless MCU module series based on TI's SimpleLink™ Wi-Fi System-on-Chip CC3551. This module series is ideal for cost-sensitive embedded applications with RTOS software, where the peak application throughput requirement is a maximum of 20 Mbps. The BDE-BW3551 module series is an excellent choice for bringing the efficiency of Wi-Fi 6 to embedded device applications for the Internet of Things (IoT), featuring a small PCB footprint and a highly optimized bill of materials for lower costs. Additionally, the module is backward compatible with Wi-Fi 4 (802.11 b/g/n) and Wi-Fi 5 (802.11 ac).

In order to fulfill different integration requirements, BDE offers various variants. These are listed in Table 1.

Table 1. Module Variants

Model Series	Orderable Part Number	Connectivity	Flash (MB)	Optional PSRAM (MB)	Antenna Options
BDE-BW355	BDE-BW3551A40	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	0	PCB trace antenna
	BDE-BW3551A80	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	0	
	BDE-BW3551A160	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	0	
	BDE-BW3551A42	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	2	
	BDE-BW3551A82	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	2	
	BDE-BW3551A162	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	2	
	BDE-BW3551A48	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	8	
	BDE-BW3551A88	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	8	
	BDE-BW3551A168	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	8	
	BDE-BW3551U40	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	0	U.FL connector
	BDE-BW3551U80	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	0	
	BDE-BW3551U160	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	0	
	BDE-BW3551U42	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	2	
	BDE-BW3551U82	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	2	
	BDE-BW3551U162	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	2	
	BDE-BW3551U48	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	8	
	BDE-BW3551U88	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	8	
	BDE-BW3551U168	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	8	
	BDE-BW3551N40	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	0	ANT pin
	BDE-BW3551N80	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	0	

Model Series	Orderable Part Number	Connectivity	Flash (MB)	Optional PSRAM (MB)	Antenna Options
	BDE-BW3551N160	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	0	
	BDE-BW3551N42	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	2	
	BDE-BW3551N82	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	2	
	BDE-BW3551N162	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	2	
	BDE-BW3551N48	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	4	8	
	BDE-BW3551N88	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	8	8	
	BDE-BW3551N168	2.4-GHz & 5-GHz Wi-Fi 6 SISO and BLE	16	8	

Key Features

Microcontroller

- Powerful 160MHz Arm® Cortex®-M33 processor with FPU, TrustZone®, and AI acceleration
- High-speed Quad-SPI XiP flash with on-the-fly decryption
- Flexible configuration of low-latency TCM (up to 32KB) and Cache (32KB or 64KB) for improved code execution performance
- Over 1MB embedded SRAM including 128KB TCM for Wi-Fi, BLE, networking, and application data
- Support for additional external PSRAM

Peripherals

- Up to 29 I/Os with flexible multiplexing options
- 8 x General-Purpose Timers / Pulse-Width Modulation (PWM)
- 2 x Universal Asynchronous Receiver-Transmitter (UART)
- 2 x Serial Peripheral Interface (SPI)
- 2 x Inter-Integrated Circuit (I2C)
- Inter-IC Sound (I2S)
- Pulse Density Modulation (PDM)
- Secure Digital / Multimedia Card (SD/MMC)
- Secure Digital Input Output (SDIO) 2.0
- Controller Area Network (CAN) 2.0
- 8 channel, 12-bit Analog to Digital Converter
- (ADC)

System Services

- Direct Memory Access (DMA)
- One-time-programmable memory (OTP)
- Real-time clock (RTC) and Watchdog Timer (WDT)

Radio

- 2.4GHz & 5GHz dual-band Wi-Fi 6 (802.11ax)
  - Single-stream 20-MHz channels with application throughput up to 20Mbps (UDP)
  - Compatible with IEEE 802.11 b/g/n/ax
    - Orthogonal Frequency-Division Multiple Access (OFDMA)
    - Target Wake Time (TWT)
    - Trigger Frames
    - Basic Service Set (BSS) Color
  - Integrated PA for complete WLAN Solution with up to 18 dBm output power at 1 DSSS
  - Role support: STA, softAP with up to 4 stations, Wi-Fi Direct, Multi-role AP + STA
  - Support for Personal and Enterprise Wi-Fi Security: WPA / WPA2 PSK, WPA2 Enterprise, WPA3 Personal or Enterprise
  - Wi-Fi TX Power
    - 18 dBm at 1 DSSS
    - 16 dBm at 54 OFDM
  - Wi-Fi RX Sensitivity
    - -96 dBm at 1 DSSS
    - -73 dBm at 54 OFDM
- Bluetooth® Low Energy
  - Bluetooth low energy 5.4 certified stack
  - Supports long-range and high-speed PHYs (up to 2 Mbps)

Security Features

- ARM TrustZone
- Hardware Security Module supporting all of the following:
  - ECC, RSA, AES, SHA2/3, MD5, CRC 16/32, and TRNG
  - Secure key storage

- Initial Secure Programming
- Secure Boot
- Software IP and Cloning Protection
- Debug security through JTAG and Debug port lock
- OTP with ability to program root-of-trust public key
- Secure Over-the-Air (OTA) updates
- Anti-rollback protection

Other Features

- Support for 3-wire PTA coexistence interface for use with external 2.4GHz radios (for example Thread or Zigbee®)
- Antenna selection capability
- Operating temperature: -40°C to +85°C
- Power management
  - VDD_3V3: 3 V – 3.6 V
  - VDD_1V8: 1.62V – 1.98V
  - VDD_SF: 1.8V / 3.3V
  - VDD_VIO1: 1.8V / 3.3V
  - VDD_VIO2: 1.8V / 3.3V
- Clock source
  - On-board 52 MHz XTAL fast clock
  - External 32.768-kHz oscillator
- Antenna options
  - U.FL connector for external antenna
  - Integrated PCB trace antenna
  - ANT pin for external antenna
- Package
  - LGA-68, 14mm x 14mm x 2mm
  - LGA-68, 14mm x 19mm x 2mm
  - LGA-68, 14mm x 19mm x 2mm
- Regulatory compliance (Planed)
  - FCC ID: 2ABRU-BW355
  - IC: 25657- BW355
  - CE-RED
  - MIC/TELEC

Applications

- Grid Infrastructure
  - Electricity Meter
  - String Inverter
  - Micro Inverter
  - Energy Storage Power Conversion System (PCS)
  - EV Charging Infrastructure
- Building and Home Automation
  - HVAC Controller
  - HVAC Gateway
  - Thermostat
  - Building Security Gateway
  - Garage Door System
  - IP Network Camera/ Video Doorbell
  - Wireless Security Camera
- Appliances
  - Refrigerator & Freezer
  - Oven
  - Washer & Dryer
  - Residential Water Heater & Heating System
  - Air Purifier & Humidifier
  - Coffee Machine
  - Air Conditioner Indoor Unit
  - Vacuum Robot
  - Robotic Lawn Mower
- Medical
  - Infusion Pump
  - Electronic Hospital Bed & Bed Control
  - Multiparameter Patient Monitor
  - Blood Pressure Monitor
  - CPAP Machine
  - Telehealth Systems
  - Ultrasound Scanner
  - Ultrasound Smart Probe
  - Electric Toothbrush
- Retail Automation and Payment
- Printers

Contents

List of Tables

List of Figures

References

1. CC3551 resources: https://www.ti.com/product/CC3551E;

1. System Overview

1.1. Block Diagram

BDE-BW3551 module series is based on the TI's SimpleLink™ Wi-Fi System-on-Chip CC3551. The module series, as seen in below diagrams, depending on different configurations, comprises of:

- 52-MHz XTAL
- Bandpass filter
- *Quad-SPI nor flash, different memory size depending on the variants
- *Quad-SPI PSRAM, different memory size depending on the variants
- Decoupling capacitors
- U.FL connector (U variants)
- PCB trace antenna (A variants)

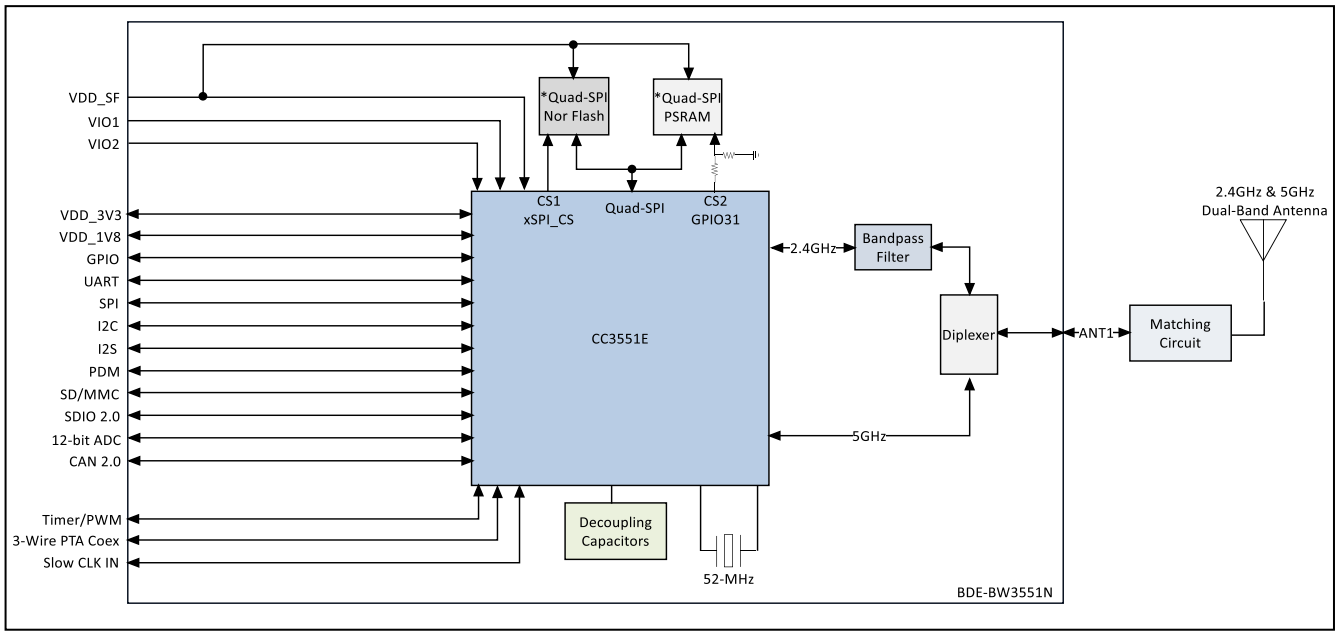


Figure 1. The block diagram of BDE-BW3551N

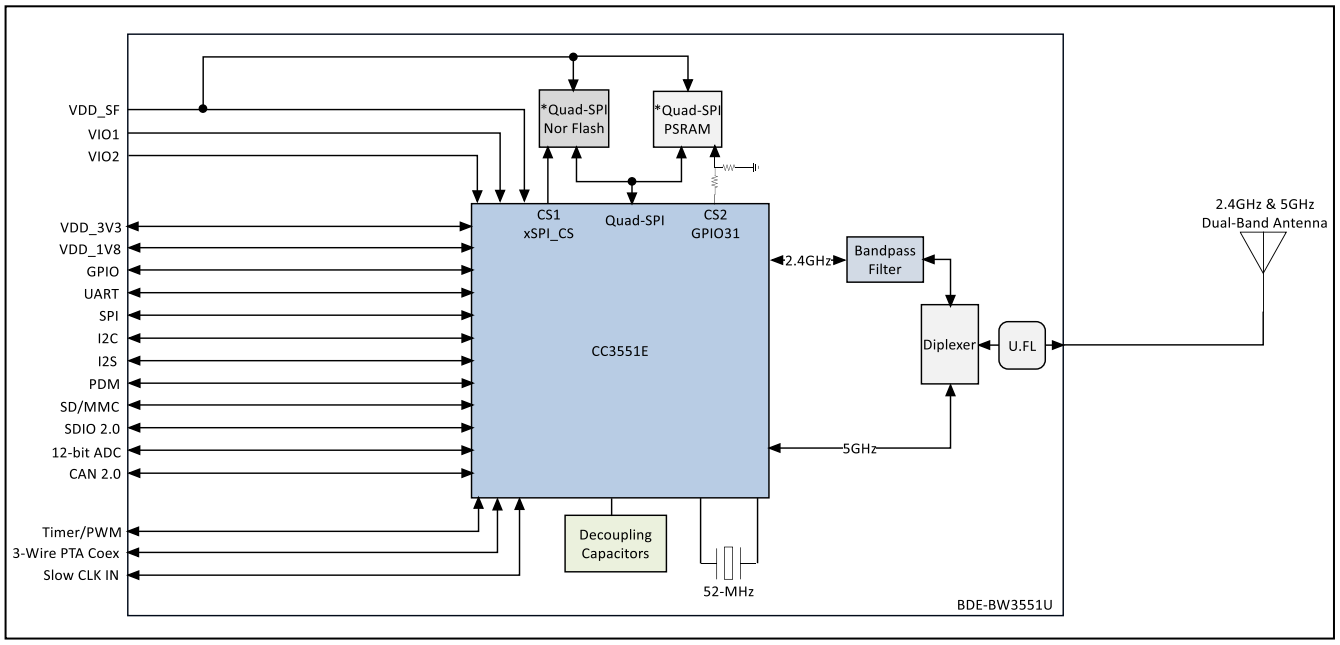


Figure 2. The block diagram of BDE-BW3551U

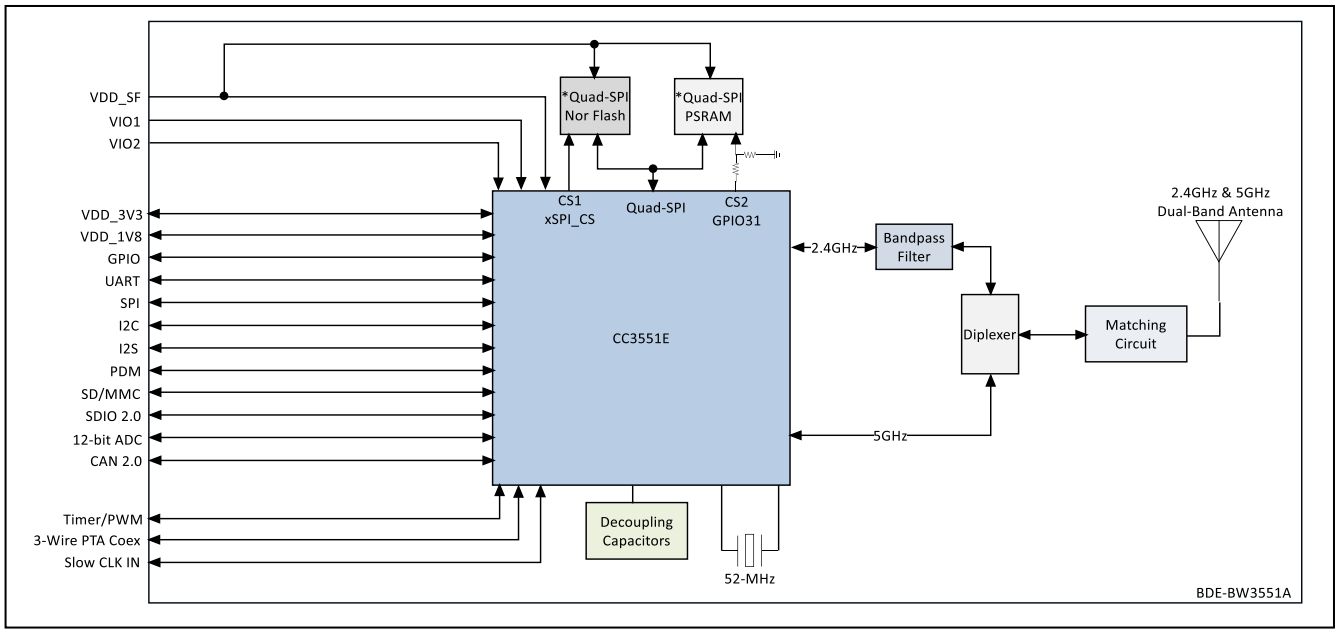


Figure 3. The block diagram of BDE-BW3551A

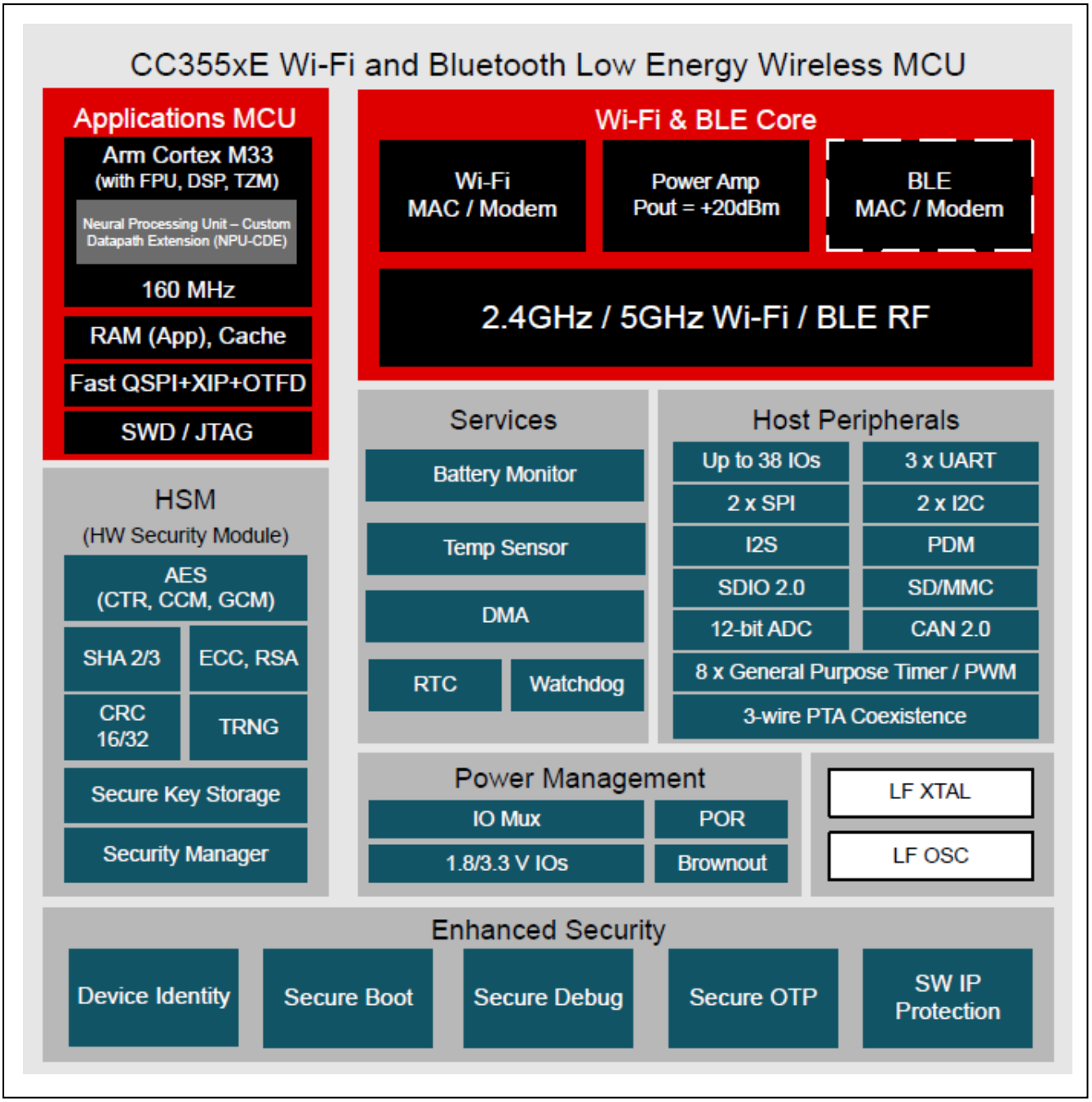


Figure 4. The block diagram of CC355x (Adopted form CC355x Datasheet)

2. Pinout Functions

2.1. Pin Diagram

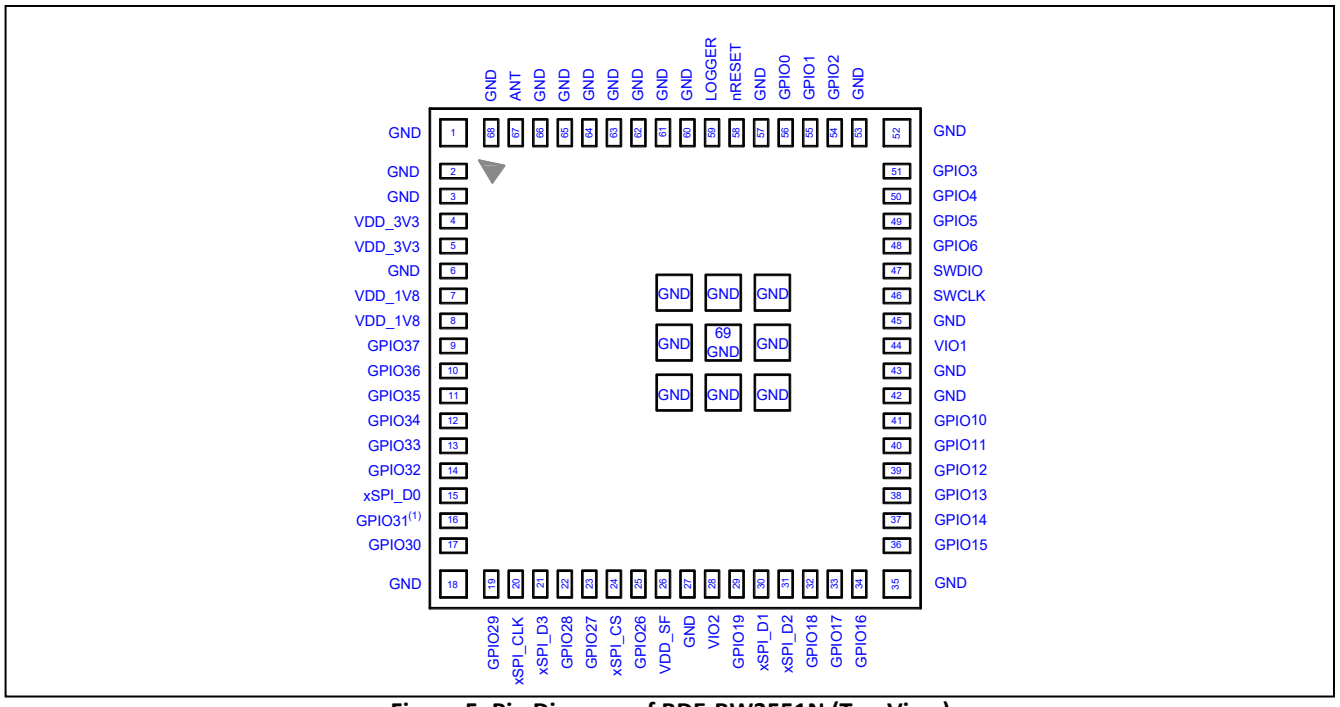


Figure 5. Pin Diagram of BDE-BW3551N (Top View)

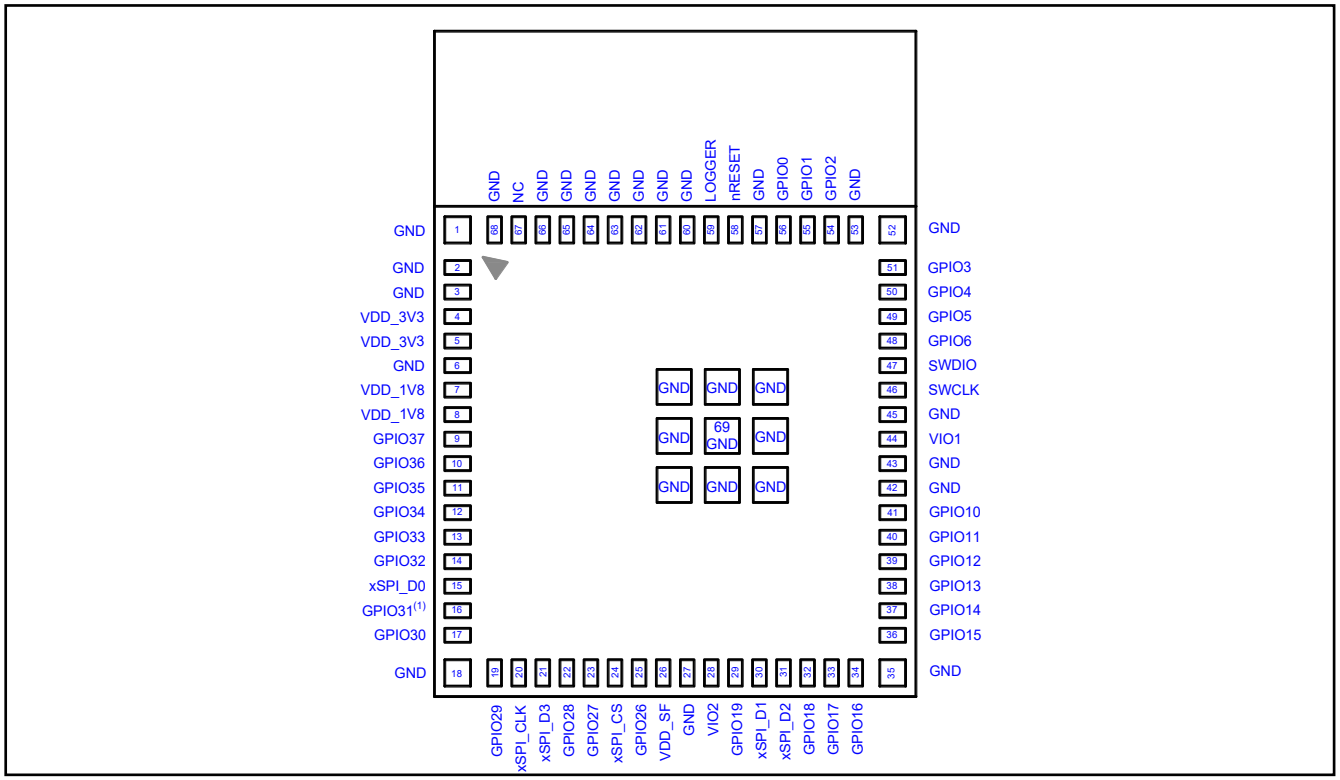


Figure 6. Pin Diagram of BDE-BW3551A and BDE-BW3351U (Top View)

(1) GPIO31 is used as the chip select signal of PSRAM. Leave floating with PSRAM vagrants. Refer to Table 1 for more information on the variants.

2.2. Pinout Description

Table 2. Pinout Description

Module Pin #	Pin Name	Signal Name	Type (1)	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS (2)
1	GND	-	Ground	-	-	-	-
2	GND	-	Ground	-	-	-	-
3	GND	-	Ground	-	-	-	-
4	VDD_3V3	-	Power	-	-	-	-
5	VDD_3V3	-	Power	-	-	-	-
6	GND	-	Ground	-	-	-	-
7	VDD_1V8	-	Power	-	-	-	-
8	VDD_1V8	-	Power	-	-	-	-
9	GPIO37	xSPI_CS_RAM	I/O	VIO1	1	PD	Hi-Z, Pull, Drive
		SDMMC_POW1			3		
		SDMMC_WP			4		
		COEX_REQ			18		
		SDIO_OOB_IRQ			19		
		COEX_GRANT			20		
		ANT_SEL_0			23		
		CCA			24		
10	GPIO36	xSPI_CS_RAM	I/O	VIO1	1	PD	Hi-Z, Pull, Drive
		SDMMC_POW2			3		
		SDMMC_WP			4		
		COEX_REQ			19		
		COEX_GRANT			20		
		CCA			24		
11	GPIO35	xSPI_Reset_Flash	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI1_CLK			3		
		xSPI_Reset_RAM			4		
		UART1_RX			5		
		I2C0_DATA			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT0_1			9		
		DCAN_RX			10		
		I2C1_DATA			11		
		xSPI_CS_RAM			12		
		SPI0_CS4			16		
		SPI0_CS3			17		
		GPT0_2_N			18		
		GPT1_2_N			19		
		COEX_PRIORITY			20		
		ANT_SEL_0			23		
		GPT1_PRE_EVENT			24		
		xSPI_DQS			28		
		COEX_REQ			29		
		SDIO_CMD			30		
12	GPIO34	xSPI_RESET_RAM	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI1_PICO			4		
		UART1_CTS			5		
		I2C1_DATA			6		
		I2S_BCLK			7		
		PDM_DATA1			8		
		GPT1_3			9		
		DCAN_RX			10		
		SPI0_CS2			16		
		GPT1_1_N			18		
		GPT0_3_N			19		
		COEX_REQ			20		
		SDIO_CLK			30		
13	GPIO33	SPI1_POCI	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART1_RX			5		
		I2C0_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_2			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_0_N			18		

Module Pin #	Pin Name	Signal Name	Type [1]	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS [2]
		GPT0_2_N			19		
		COEX_GRANT			20		
		GPT1_PRE_EVENT			24		
		SDIO_D0			30		
14	GPIO32	xSPI_CS_RAM	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI1_CS1			3		
		SPI1_CLK			4		
		UART1_TX			5		
		I2C0_DATA			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT1_1			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		GPT1_0_N			18		
		GPT0_1_N			19		
		COEX_REQ			20		
		SDIO_D1			30		
15	xSPI_D0[3]	xSPI_D0	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
16	GPIO31[4]	xSPI_CS_RAM	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		xSPI_RESET_RAM			3		
		SPI1_CS1			4		
		UART1_RTS			5		
		I2C1_CLK			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT1_0			9		
		DCAN_TX			10		
		SPI0_CS3			16		
		GPT1_1_N			18		
		GPT0_0_N			19		
		COEX_GRANT			20		
		ANT_SEL_0			23		
		GPT_INFRARED			24		
		SDIO_D2			30		
17	GPIO30	xSPI_DQS	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		xSPI_RESET_FLASH			3		
		xSPI_RESET_RAM			4		
		I2C1_CLK			5		
		I2C0_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_1			9		
		DCAN_TX			10		
		xSPI_CS_RAM			12		
		SPI0_CS2			16		
		GPT0_2_N			18		
		COEX_GRANT			19		
		COEX_REQ			20		
		ANT_SEL_0			23		
		CCA			24		
		GPT1_PRE_EVENT			28		
		GPT0_PRE_EVENT			29		
		SDIO_D3			30		
18	GND	-	Ground	-	-	-	-
19	GPIO29	xSPI_DATA_7	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI0_PICO			4		
		UART0_CTS			5		
		I2C1_DATA			6		
		I2S_BCLK			7		
		PDM_DATA1			8		
		GPT0_3			9		
		DCAN_RX			10		
		I2S_MCLK			12		
		SPI1_CS4			16		
		GPT0_1_N			18		
		GPT1_3_N			19		
		COEX_GRANT			20		
		SDIO_OOB_IRQ			30		
20	xSPI_CLK[3]	xSPI_CLK	O	VDD_SF	-	PU	Hi-Z, Pull, Drive

Module Pin #	Pin Name	Signal Name	Type [1]	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS [2]
21	xSPI_D3[3]	xSPI_D3	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
22	GPIO28	xSPI_DATA_6	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI0_POCI			4		
		UART0_RX			5		
		I2C0_CLK			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT0_2			9		
		SPI1_CS4			16		
		GPT0_0_N			18		
		GPT1_2_N			19		
		COEX_PRIORITY			20		
		GPT0_PRE_EVENT			24		
23	GPIO27	xSPI_DATA_5	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI0_CLK			4		
		UART0_TX			5		
		I2C0_DATA			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT0_1			9		
		SPI1_CS3			16		
		GPT0_0_N			18		
		GPT1_1_N			19		
		COEX_REQ			20		
24	xSPI_CS[5]	xSPI_CS	O	VDD_SF	-	PU	1
25	GPIO26	xSPI_DATA_4	I/O	VIO2	1	PU	Hi-Z, Pull, Drive
		SPI0_CS1			4		
		UART0_RTS			5		
		I2C1_CLK			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT0_0			9		
		DCAN_TX			10		
		SPI1_CS2			16		
		GPT0_1_N			18		
		GPT1_0_N			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		ANT_SEL_0			23		
		GPT_INFRARED			24		
		SDIO_OOB_IRQ			30		
26	VDD_SF[6]	-	Power	-	-	-	-
27	GND	-	Ground	-	-	-	-
28	VIO2[6]	-	Power	-	-	-	-
29	GPIO19	SPI0_PICO	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_CTS			5		
		I2C1_CLK			6		
		I2S_BCLK			7		
		PDM_DATA0			8		
		GPT0_3			9		
		DCAN_RX			10		
		GPT0_PRE_EVENT			16		
		SDIO_OOB_IRQ			17		
		GPT0_1_N			18		
		SDIO_D3			19		
		COEX_PRIORITY			20		
		GPT1_3_N			21		
		GPT_INFRARED			22		
30	xSPI_D1[3]	xSPI_D1	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
31	xSPI_D2[3]	xSPI_D2	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
32	GPIO18	SPI0_POCI	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_RX			5		
		I2C0_DATA			6		
		I2S_DATA0			7		
		PDM_DATA1			8		
		GPT0_2			9		
		DCAN_TX			10		
		SPI1_CS4			16		
		SDIO_OOB_IRQ			17		
		GPT0_0_N			18		

Module Pin #	Pin Name	Signal Name	Type [1]	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS [2]
		COEX_REQ			20		
		GPT1_2_N			21		
33	GPIO17	SDMMC_WP	I/O	VIO1	1	PU	Hi-Z, Pull, Drive
		SPI0_CLK			4		
		UART0_TX			5		
		I2C0_CLK			6		
		I2S_DATA1			7		
		PDM_DATA0			8		
		GPT0_1			9		
		SPI1_CS3			16		
		SDIO_OOB_IRQ			17		
		GPT0_0_N			18		
		COEX_GRANT			20		
		GPT1_1_N			21		
34	GPIO16	SPI0_CS1	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_RTS			5		
		I2C1_DATA			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT0_0			9		
		SPI1_CS2			16		
		GPT0_1_N			18		
		SDIO_D2			19		
		GPT1_0_N			21		
		GPT_INFRARED			22		
		ANT_SEL_0			23		
35	GND	-	Ground	-	-	-	-
36	GPIO15	SDMMC_CMD	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_POCI			4		
		UART1_RX			5		
		UART0_CTS			6		
		GPT1_1			9		
		SPI0_CS2			16		
		GPT0_PRE_EVENT			17		
		GPT1_0_N			18		
		SDIO_D1			19		
		COEX_REQ			20		
37	GPIO14	SDMMC_CLK	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_CLK			4		
		UART1_TX			5		
		UART0_RX			6		
		GPT1_0			9		
		SPI0_CS2			16		
		GPT1_PRE_EVENT			17		
		GPT1_1_N			18		
		SDIO_D0			19		
		COEX_GRANT			20		
38	GPIO13	SDMMC_DATA_0	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_PICO			4		
		UART1_CTS			5		
		UART0_TX			6		
		I2S_BCLK			7		
		I2S_MCLK			8		
		GPT1_3			9		
		GPT1_2_N			18		
		SDIO_CMD			19		
		COEX_PRIORITY			20		
		ANT_SEL_0			23		
39	GPIO12	SDMMC_DATA_1	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_CS1			4		
		UART1_RTS			5		
		UART0_RTS			6		
		I2S_WCLK			7		
		GPT1_2			9		
		GPT0_PRE_EVENT			16		
		GPT1_PRE_EVENT			17		
		GPT1_3_N			18		
		SDIO_CLK			19		
40	GPIO11	ADC0	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_RX			1		

Module Pin #	Pin Name	Signal Name	Type [1]	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS [2]
		SDMMC_DATA_2			3		
		SPI1_CS1			4		
		UART1_CTS			5		
		I2C1_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_1			9		
		DCAN_TX			10		
		SPI0_CS2			16		
		GPT1_2_N			18		
		SDIO_D2			19		
		COEX_REQ			20		
		CCA			24		
41	GPIO10	ADC1	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_TX			1		
		SDMMC_DATA_3			3		
		SPI1_CLK			4		
		UART1_RTS			5		
		I2C1_DATA			6		
		I2S_DATA1			7		
		PDM_DATA1			8		
		GPT1_0			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		GPT1_3_N			18		
		SDIO_D3			19		
		COEX_PRIORITY			20		
		COEX_GRANT			21		
		CCA			24		
42	GND	-	Ground	-	-	-	-
43	GND	-	Ground	-	-	-	-
44	VIO1[6]	-	Power	-	-	-	-
45	GND	-	Ground	-	-	-	-
46	SWCLK	SWCLK	O	VIO1	-	PD	Hi-Z, Pull, Drive
47	SWDIO	SWDIO	I/O	VIO1	-	PU	Hi-Z, Pull, Drive
48	GPIO6	ADC2	I/O	VIO1		PU	Hi-Z, Pull, Drive
		xSPI_CS_RAM			1		
		SDMMC_POW1			3		
		SPI1_PICO			4		
		UART1_RX			5		
		I2C0_DATA			6		
		I2S_WCLK			7		
		PDM_DATA0			8		
		GPT1_3			9		
		DCAN_RX			10		
		SDMMC_WP			11		
		SPI0_CS4			16		
		I2S_BCLK			17		
		GPT1_1_N			18		
		SDIO_D1			19		
		COEX_PRIORITY			20		
		GPT0_3_N			21		
		GPT1_PRE_EVENT			22		
		ANT_SEL_0			23		
		CCA			24		
		COEX_GRANT			26		
		I2C1_CLK			28		
		SDMMC_POW2			29		
49	GPIO5	ADC3	I/O	VIO1		PU	Hi-Z, Pull, Drive
		xSPI_RESET_RAM			1		
		SDMMC_POW2			3		
		SPI1_POCI			4		
		UART1_TX			5		
		I2C0_CLK			6		
		I2S_MCLK			7		
		PDM_BCLK			8		
		GPT1_2			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_0_N			18		

Module Pin #	Pin Name	Signal Name	Type [1]	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS [2]
		SDIO_D0			19		
		COEX_REQ			20		
		GPT0_2_N			21		
		I2C1_DATA			28		
50	GPIO4	ADC4	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_RX			1		
		SDMMC_CD			3		
		SPI1_CS1			4		
		UART1_CTS			5		
		I2S_BCLK			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT1_1			9		
		DCAN_TX			10		
		SPI0_CS2			16		
		GPT1_0_N			18		
		SDIO_CMD			19		
		COEX_PRIORITY			20		
		GPT0_1_N			21		
		I2C1_CLK			28		
51	GPIO3	ADC5	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_TX			1		
		SDMMC_WP			3		
		SPI1_CLK			4		
		UART1_RTS			5		
		I2S_MCLK			6		
		I2S_DATA0			7		
		PDM_DATA1			8		
		GPT1_0			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		xSPI_CS_RAM			17		
		GPT1_1_N			18		
		SDIO_CLK			19		
		COEX_REQ			20		
		GPT0_0_N			21		
		GPT_INFRARED			22		
		I2C1_DATA			28		
52	GND	-	Ground	-	-	-	-
53	GND	-	Ground	-	-	-	-
54	GPIO2	ADC6	I/O	VIO1		PU	Hi-Z, Pull, Drive
		xSPI_RESET_RAM			1		
		SDMMC_CD			3		
		I2C1_CLK			6		
		GPT1_3			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_PRE_EVENT			18		
		SDIO_OOB_IRQ			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		CCA			24		
55	GPIO1	LFXTAL_N	I/O	VIO1	0	PD	Hi-Z, Pull, Drive
		ADC7					
		GPT1_PRE_EVENT			7		
		GPT0_PRE_EVENT			8		
		GPT1_0			9		
		GPT0_0			10		
		GPT_INFRARED			11		
		SDIO_OOB_IRQ			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		ANT_SEL_0			23		
56	GPIO0	LFXTAL_P	I/O	VIO1		PD	Hi-Z, Pull, Drive
		SLOW_CLK_IN			1		
		GPT1_1			9		
		GPT0_1			10		
		COEX_REQ			21		
57	GND	-	Ground	-	-	-	-
58	nRESET	nRESET	I	-	-	-	-

Module Pin #	Pin Name	Signal Name	Type (1)	IO Ring	Pin Mux Encoding	Pad States	
						Reset	LPDS (2)
59	LOGGER	LOGGER	O	VIO1	-	PU	Hi-Z, Pull, Drive
60	GND	-	Ground	-	-	-	-
61	GND	-	Ground	-	-	-	-
62	GND	-	Ground	-	-	-	-
63	GND	-	Ground	-	-	-	-
64	GND	-	Ground	-	-	-	-
65	GND	-	Ground	-	-	-	-
66	GND	-	Ground	-	-	-	-
67	ANT(7)	ANT	RF	-	-	-	-
68	GND	-	Ground	-	-	-	-
69	GND, thermal pads	-	Ground	-	-	-	-

(1) Signal Types: I = Input, O = Output, I/O = Input or Output;
(2) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need;
(3) xSPI_D0, xSPI_D1, xSPI_D2, xSPI_D3, xSPI_CLK are for on-module SFLASH and PSRAM;
(4) GPIO31 is for chip select signal for on-module PSRAM;
(5) xSPI_CS is for chip select signal for on-module SFLASH;
(6) VDD_SF, VIO1, VIO2 can be supplied with 3.3V or 1.8V;
(7) The ANT pin is used in BDE-BW3551N, leave floating in BDE-BW3551U and BDE-BW3551A.

3. Characteristics

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	MIN	MAX	Unit
VDD_3V3	-0.5	4.2	V
VDD_1V8	-0.5	2.1	V
VIO1	-0.5	3.6	V
VIO2	-0.5	3.6	V
VDD_SF	-0.5	3.6	V
Operating ambient temperature	-40	105	°C
Storage temperature	-40	105	°C

3.1.2. ESD Ratings

Table 4. ESD Ratings

Parameter	Description	Value	Unit	Note
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

3.1.3. Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	MIN	TYP	MAX	Unit
VDD_3V3	3	3.3	3.6	V
VDD_1V8	1.62	1.8	1.98	V
VIO1	1.62/3	1.8/3.3	1.98/3.6	V
VIO2	1.62/3	1.8/3.3	1.98/3.6	V

VDD_SF	1.62/3	1.8/3.3	1.98/3.6	V
Operating ambient temperature	-40		85	℃

3.1.4. I/O DC Characteristics

Table 6. I/O DC Characteristics

Parameter	Description	Test Condition	MIN	MAX	Unit
V_{IH}	High level input voltage		0.65 x VIO	VIO1/VIO	V
V_{IL}	Low level input voltage		0	0.35 x VIO	
V_{OH}	High level output voltage	at 4mA	VIO – 0.45	VIO	
V_{OL}	Low level output voltage	at 4mA	0	0.45	
$V_{IH\ nRESET}$	High level input voltage, nRESET pin		1.35	3.3	
$V_{IL\ nRESET}$	Low level input voltage, nRESET pin		0	0.45	

(1) The VIO can be the VIO1 or VIO2, which can be set to either 1.8 or 3.3V.

3.1.5. Power Consumption

Table 7. Current Consumption – WLAN 2.4-GHz Static Modes

Parameter	Test Condition		TYP	Unit
Continuous TX (1)	1 DSSS	TX power = 18.6 dBm	356	mA
	6 OFDM	TX power = 18.6 dBm	354	
	54 OFDM	TX power = 16.1 dBm	309	
	HT MCS0	TX power = 18.6 dBm	354	
	HT MCS7	TX power = 16.1 dBm	310	
	HE MCS0	TX power = 18.6 dBm	365	
	HE MCS7	TX power = 15.9 dBm	310	
Continuous RX			68	

Table 8. Current Consumption – WLAN 2.4-GHz Use Cases

Mode	Description	TYP	Unit
DTIM = 1	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~100ms)	1617	µA
DTIM = 3	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=3 (~300ms)	941	
DTIM = 5	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=5 (~500ms)	809	

Table 9. Current Consumption – WLAN 5-GHz Static Modes

Parameter	Test Condition		TYP	Unit
Continuous TX	6 OFDM	TX power = 18.0 dBm	405	mA
	54 OFDM	TX power = 13.7 dBm	372	
	HT MCS0	TX power = 18.1 dBm	418	
	HT MCS7	TX power = 13.5 dBm	347	
	HE MCS0	TX power = 18.2 dBm	401	
	HE MCS7	TX power = 12.1 dBm	339	
Continuous RX			108	

Table 10. Current Consumption – WLAN 5-GHz Use Cases

Mode	Description	TYP	Unit
DTIM = 1	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=1 (~100ms)	1865	µA
DTIM = 3	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=3 (~300ms)	990	
DTIM = 5	System with 3.3V to Ext. DC/DC at 85% efficiency WLAN beacon reception every DTIM=5 (~500ms)	860	

Table 11. Current Consumption – Device States

Mode	Description	TYP	Unit
Shutdown	External supplies are available, device held in reset (nRESET is low)	TBD	µA
Sleep	Low power mode – RAM in retention	TBD	

3.1.6. Fast Clock Characteristics

The fast clock running at 52-MHz for WLAN functions is included in the module. The specification is shown in below table.

Table 12. 52-MHz Crystal Oscillator (HFXT) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			52		MHz
ESR, Equivalent series resistance				20	Ω
Frequency tolerance	T_A: 25°C	-10		+10	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			8		pF

3.1.7. External Slow Clock Requirements

The slow clock running at 32.768-KHz for low power modes is not included in the module. The slow clock can be generated internally by the IC or externally either by using an oscillator or a XTAL or a source from the system.

If using an oscillator or the source from the system, the slow clock must meet the requirements listed in below table. This clock should be fed into the module pin 56 (GPIO0) and should be stable before nRESET is deasserted and device is enabled. The clock signal logic high should be the same voltage as VIO1 IO Ring.

Table 13. External 32.768-KHz Slow Clock Requirements

Parameter	Description	MIN	TYP	MAX	Unit
Crystal frequency	Square wave		32768		Hz
Frequency accuracy	Initial + temperature + aging	-250		+250	ppm
Input duty cycle		30	50	70	%
Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
Input low level		0		0.35 x VIO1	V
Input high level		0.65 x VIO1		3.6	V
Input impedance		1			MΩ
Input capacitance				5	pF

The slow clock of module can also be sourced by the external XTAL. The crystal pins should be fed into the module pin 55 (GPIO1/LFXT_N) and pin 56 (GPIO0/LFXT_P). The specification of the XTAL is listed in below table.

Table 14. External 32.768-KHz XTAL (LFXT) Requirements

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32.768		KHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-20		+20	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			12.5		pF

3.2. RF Characteristics

3.2.1. WLAN Performance: 2.4-GHz Receiver Characteristics

Table 15. WLAN Performance: 2.4-GHz Receiver Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Operational frequency range		2412		2472	MHz
Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 DSSS		-96		dBm
	2 DSSS		-93		
	11 DSSS		-88		
	6 OFDM		-91		
	54 OFDM		-73		
	HT MCS0 MM 4K		-91		
	HT MCS7 MM 4K		-70		
	HE MCS0 4K		-90		
	HE MCS7 4K		-70		
Maximum input level: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 DSSS		0		dBm
	6 OFDM, HT MCS0, HE MCS0		0		
	54 OFDM, HT MCS7, HE MCS7		-9		
Adjacent channel rejection	1 DSSS		45		dB
	2 DSSS		39		
	11 DSSS		20		
	6 OFDM		3		
	54 OFDM		20		
	HT MCS0 MM 4K		3		
	HT MCS7 MM 4K		16		
	HE MCS0 4K		-1		
RSSI accuracy	-90 dBm to -30 dBm	-3		3	dB

3.2.2. WLAN Performance: 2.4-GHz Transmitter Characteristics

Table 16. WLAN Performance: 2.4-GHz Transmitter Power

Parameter	Test Condition	MIN	TYP	MAX	Unit
Operational frequency range		2412		2472	MHz
Output power at VDD_3V3 = 3.3 V	1 DSSS		18		dBm
	6 OFDM		18		
	54 OFDM		16		
	HT MCS0 MM 4K		17		
	HT MCS7 MM 4K		16		
	HE MCS0 4K		18		
	HE MCS7 4K		16		

(2) The output power is measured at frequency 2437MHz;
(3) Typical power is the average power, peak power can reach 24 dBm.

3.2.1. WLAN Performance: 5-GHz Receiver Characteristics

Table 17. WLAN Performance: 5-GHz Receiver Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Operational frequency range		5180		5845	MHz
Sensitivity: 10% PER for 11g/n/ax rates	6 OFDM		-92		
	54 OFDM		-74.5		
	HT MCS0 MM 4K		-92		
	HT MCS7 MM 4K		-71.5		
	HE MCS0 4K		-91.5		
	HE MCS7 4K		-70		
Maximum input level: 10% PER for 11g/n/ax rates	6 OFDM, HT MCS0, HE MCS0		-23		dBm
	54 OFDM, HT MCS7, HE MCS7		-24		
Adjacent channel rejection	6 OFDM		20		dB
	54 OFDM		3		
	HT MCS0		18		
	HT MCS7		0		
	HE MCS0		16		
	HE MCS7		-1		
RSSI accuracy	-90 dBm to -30 dBm	-3		3	dB

3.2.2. WLAN Performance: 5-GHz Transmitter Characteristics

Table 18. WLAN Performance: 5-GHz Transmitter Power

Parameter	Test Condition	MIN	TYP	MAX	Unit
Operational frequency range		5180		5845	MHz
Output power at VDD_3V3 = 3.3 V	6 OFDM		18.2		dBm
	54 OFDM		13.5		
	HT MCS0		18.1		
	HT MCS7		13.5		
	HE MCS0		18.1		
	HE MCS7		12.3		

(1) The output power is measured at frequency 5580MHz. Measurements on other channels may show a variance of 1 to 2 dB. Typical power was recorded as average power, peak power can reach 20 dBm. TX power on each channel might be limited by the regulatory requirement.

3.2.3. BLE Performance: Receiver Characteristics

Table 19. BLE Performance: 2.4-GHz Receiver Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
BLE 125Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.8%		-102		dBm
Receiver saturation	PER <30.8%		0		
Co-channel rejection (1)	Wanted signal at -79 dBm, modulated interferer in channel		10		dB
Selectivity, ±1 MHz (1)	Wanted signal at -79 dBm, modulated interferer at ±1 MHz		0 / 0 (2)		
Selectivity, ±2 MHz (1)	Wanted signal at -79 dBm, modulated interferer at ±2 MHz		-37 / -30 (2)		
Selectivity, ±3 MHz (1)	Wanted signal at -79 dBm, modulated interferer at ±3 MHz		-39 / -36 (2)		
Selectivity, ±4 MHz (1)	Wanted signal at -79 dBm, modulated interferer at ±4MHz		-45 / -41 (2)		
RSSI accuracy	-90 dBm to -20 dBm	-4		4	
BLE 500Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.8%		-99		dBm
Receiver saturation	PER <30.8%		0		
Co-channel rejection (1)	Wanted signal at -72 dBm, modulated interferer in channel		10		dB
Selectivity, ±1 MHz (1)	Wanted signal at -72 dBm, modulated interferer at ±1 MHz		0 / 0 (2)		
Selectivity, ±2 MHz (1)	Wanted signal at -72 dBm, modulated interferer at ±2 MHz		-35 / -25 (2)		
Selectivity, ±3 MHz (1)	Wanted signal at -72 dBm, modulated interferer at ±3 MHz		-40 / -37 (2)		
Selectivity, ±4 MHz (1)	Wanted signal at -72 dBm, modulated interferer at ±4MHz		-45 / -40 (2)		
RSSI accuracy	-90 dBm to -20 dBm	-4		4	
BLE 1Mbps (LE 1M) Receiver Characteristics					
Receiver sensitivity	PER <30.8%, 37-byte packets		-99		dBm
Receiver sensitivity	PER <30.8%, 255-byte packets		-98		
Receiver saturation	PER <30.8%		0		
Co-channel rejection (1)	Wanted signal at -67 dBm, modulated interferer in channel		10		dB
Selectivity, ±1 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±1 MHz		0 / 0 (2)		
Selectivity, ±2 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz		-35 / -28 (2)		
Selectivity, ±3 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±3 MHz		-38 / -32 (2)		
Selectivity, ±4 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±4MHz		-45 / -40 (2)		
Out-of-band blocking	30 MHz to 2000 MHz, wanted signal at -67 dBm		-23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, wanted signal at -67 dBm		-30		
Out-of-band blocking	2484 MHz to 2997 MHz, wanted signal at -67 dBm		-30		
Out-of-band blocking	3000 MHz to 6 GHz, wanted signal at -67 dBm		-21		
Intermodulation	Wanted signal at 2402 MHz, -64 dBm, two interferers at 2405 and 2408 MHz respectively, at the given power level		-40		
RSSI accuracy	-90 dBm to -20 dBm	-4		4	dB
BLE 2Mbps (LE 2M) Receiver Characteristics					
Receiver sensitivity	PER <30.8%, 37-byte packets		-95		dBm
Receiver saturation	PER <30.8%		0		
Co-channel rejection (1)	Wanted signal at -67 dBm, modulated interferer in channel		10		dB
Selectivity, ±2 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±1 MHz		0 / 0 (2)		
Selectivity, ±4 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz		-35 / -28 (2)		
Selectivity, ±6 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±3 MHz		-35 / -28 (2)		
Alternate channel rejection, ±8 MHz (1)	Wanted signal at -67 dBm, modulated interferer at ±8MHz		-37 / -32 (2)		
Out-of-band blocking	30 MHz to 2000 MHz, wanted signal at -67 dBm		-23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, wanted signal at -67 dBm		-30		
Out-of-band blocking	2484 MHz to 2997 MHz, wanted signal at -67 dBm		-30		
Out-of-band blocking	3000 MHz to 6 GHz, wanted signal at -67 dBm		-21		
Intermodulation	Wanted signal at 2402 MHz, -64 dBm, two interferers at 2405 and 2408 MHz respectively, at the given power level		-44		
RSSI accuracy	-90 dBm to -20 dBm	-4		4	dB

(1) Numbers given as C/I dB;
(2) X / Y, where X is +N MHz and Y is –N MHz;

3.2.4. BLE Performance: Transmitter Characteristics

Table 20. BLE Performance: Transmitter Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Operational frequency range		2402		2480	MHz
Output power	Highest setting		18.4		dBm

(1) The output power is measured at frequency 2440MHz.

4. Mechanical Specifications

4.1. Module Dimensions

The module dimensions ae shown in following figures:

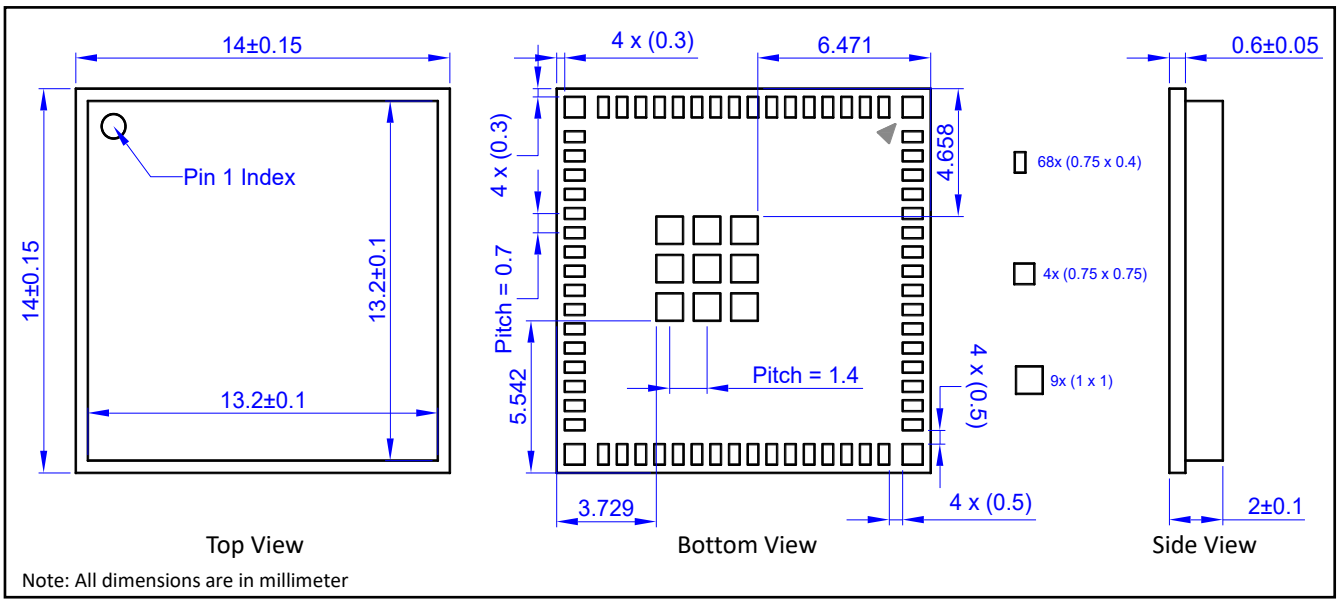


Figure 7. Mechanical Drawing of BDE-BW3551N

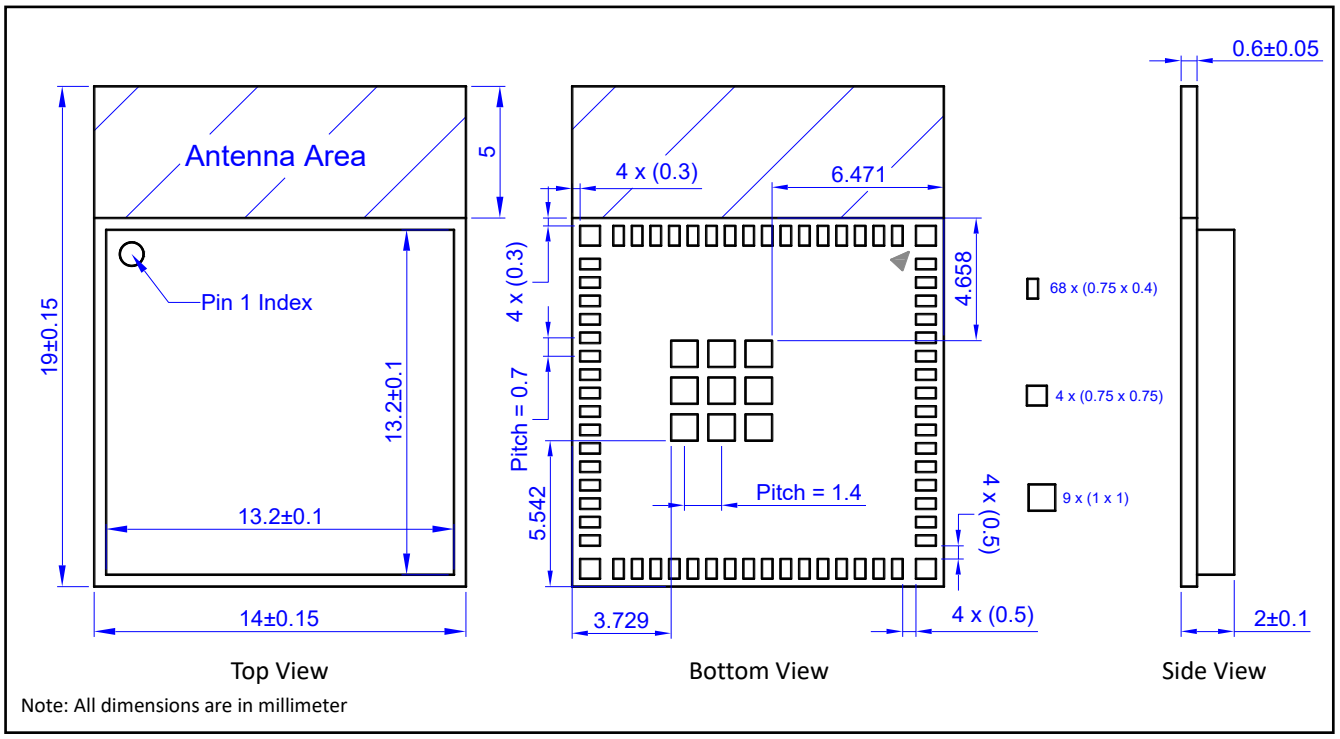
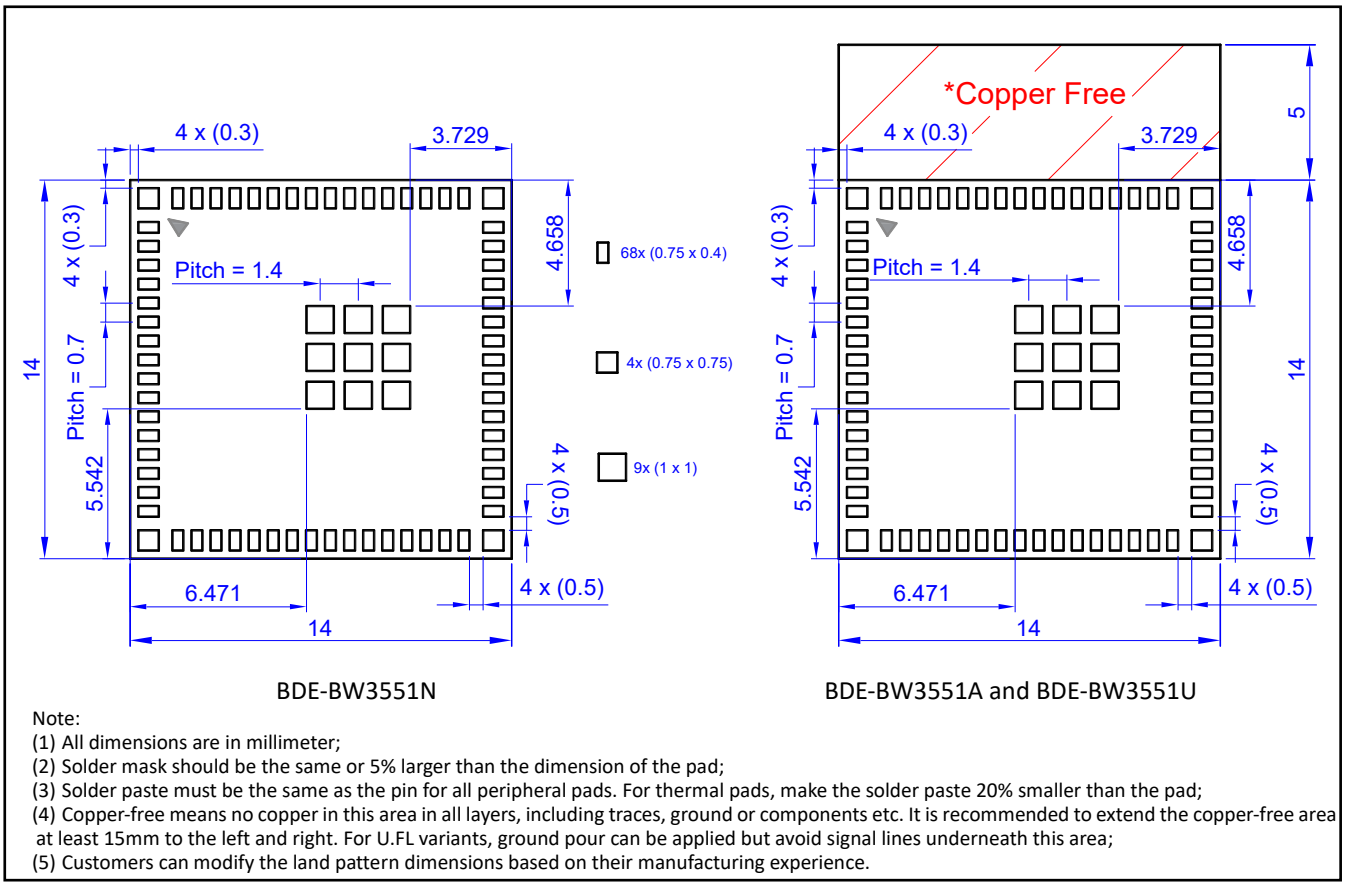


Figure 8. Mechanical Drawing of BDE-BW3551A and BDE-BW3551U

4.2. PCB Footprints

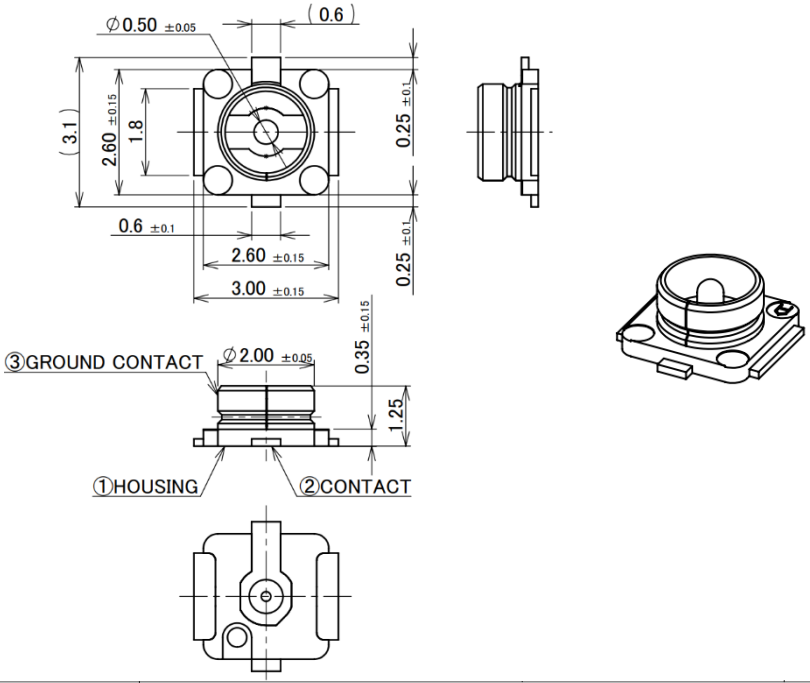


Note:
(1) All dimensions are in millimeter;
(2) Solder mask should be the same or 5% larger than the dimension of the pad;
(3) Solder paste must be the same as the pin for all peripheral pads. For thermal pads, make the solder paste 20% smaller than the pad;
(4) Copper-free means no copper in this area in all layers, including traces, ground or components etc. It is recommended to extend the copper-free area at least 15mm to the left and right. For U.FL variants, ground pour can be applied but avoid signal lines underneath this area;
(5) Customers can modify the land pattern dimensions based on their manufacturing experience.

Figure 9. Recommended Footprint Drawings

4.3. U.FL Connector Specification

The drawing and specification of the U.FL connector utilized in the module is as below for reference.
The dimension unit in below drawing is millimeter.



RATING VOLTAGE	60 V AC (R.M.S)	
RATING FREQUENCY	DC～9GHz	
OPERATING TEMPERATURE	233～363K (−40℃～+90℃)	
VSWR	RECEPTACLE: 1.3 MAX. AT 0.1～3 GHz, 1.4 MAX. AT 3～6 GHz, 1.8 MAX. AT 6～9 GHz	
MAIN CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 20 mohm MAX.	
GROUND CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 100 mohm MAX.	
INSULATION RESISTANCE	INITIAL: 500 Mohm MIN. / AFTER TEST: 100 Mohm MIN.	
DIELECTRIC WITHSTANDING VOLTAGE	200 V AC, 1 MINUTE	
DURABILITY	30 CYCLES	
UNMATING FORCE (INITIAL / AFTER TEST)	INITIAL: 5 N MIN. AFTER TEST: 3 N MIN.	INITIAL: 4 N MIN. AFTER TEST: 2 N MIN.

Figure 10. U.FL Connector Drawing and Specification

5. Revision History

Table 21. Revision History

Revision	Date	Description
V0.1	20-April-2025	Preliminary, draft, subject to change

You can find the latest datasheet on the product page at bdecomm.com.

Important Notice and Disclaimer

The information contained herein is believed to be reliable. BDE makes no warranties regarding the information contain herein. BDE assumes no responsibility or liability whatsoever for any of the information contained herein. BDE assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for BDE products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.

Contact

BDE Technology Inc.

USA: 67 E Madison St, # 1603A, Chicago, IL 60603, US
Tel: +1-312-379-9589

China: B2-403, 162 Science Avenue, Huangpu District, Guangzhou 510663, China
Tel: +86-20-28065335

Website: www.bdecomm.com Email: info@bdecomm.com