General Description

Note: Images are for illustrative purposes only; actual products may differ.

The BDE-SG1314R10 is a low-power Sub-1GHz wireless module series based on Texas Instruments (TI)'s single-chip wireless microcontroller (MCU) CC1314R106T0RGZ. In order to fulfil different integration scenarios, BDE provides different variants for this module series. They are listed and described in Table 1.

The BDE-SG1314R10 module series is embeded with an powerful 48-MHz Arm® Cortex®-M33 processor with TrustZone® based secure key storage, device ID and trusted functions, and it supports IEEE 802.15.4, IPv6-enabled smart objects (6LoWPAN), Wireless M-Bus, Wi-SUN, Amazon Sidewalk, mioty, and proprietary systems including TI 15.4-Stack (Sub-1GHz). The module series is optimized for low-power wireless communication and advanced sensing in building security systems, HVAC, smart meters, medical, wired networking, gateways and grid communications, home theater & entertainment, and connected peripherals markets.

The BDE-SG1314R10 has a low standby current of 0.98 µA with full RAM retention, which enables longer battery life wireless applications. The module supports +14 dBm output power with best-in-class transmit current consumption at 25.8 mA for Sub-1GHz operation. This is suitable for the long-range and low-power applications. It is featured with the Low SER (Soft Error Rate) FIT (Failure-in-time) for long operational lifetime with no disruption for industrial markets with always-on SRAM parity against corruption due to potential radiation events. The device also has an autonomous ultra-low power Sensor Controller CPU with fast wake-up capability. As an example, the sensor controller is capable of 1-Hz ADC sampling at 1.2-µA system current.

The module series has a software defined radio powered by an Arm® Cortex® M0 which allows support for multiple physical layers and RF standards. PHY and frequency switching can be done runtime through a dynamic multiprotocol manager (DMM) driver.

The module series integrates all required system-level hardware components including clocks, balun filter, other passives, and U.FL connector into a small PCB form factor. It is for easy assembly and low-cost PCB design.

The module is pre-certified with FCC, ISED, CE-RED to make easy integration and fast time-to-market for customers.

Table 1. Module Variants

Orderable Part Number	Antenna Options	On-Board SPI Flash (Mbit)	Operating Temperature
BDE-SG1314R10U32	U.FL Connector	32	-40 °C to +85 °C
BDE-SG1314R10N32	ANT Pin		
BDE-SG1314R10U0	U.FL Connector	0	
BDE-SG1314R10N0	ANT Pin		
BDE-SG1314R10U32-IN	U.FL Connector	32	-40 °C to +105 °C
BDE-SG1314R10N32-IN	ANT Pin		
BDE-SG1314R10U0-IN	U.FL Connector	0	
BDE-SG1314R10N0-IN	ANT Pin		

Key Features

- **Wireless microcontroller**
  - Powerful 48-MHz Arm® Cortex®- M33 processor with TrustZone®
  - FPU and DSP extension
  - 1024 KB flash program memory
  - 8 KB of cache SRAM
  - 256 KB of ultra-low leakage SRAM with parity for high-reliability operation
    - 32 KB of additional SRAM is available if parity is disabled
  - Dynamic multiprotocol manager (DMM) driver
  - Supports over-the-air upgrade (OTA)
- **Ultra-low power sensor controller**
  - Autonomous MCU with 4 KB of SRAM
  - Sample, store, and process sensor data
  - Fast wake-up for low-power operation
  - Software defined peripherals, capacitive touch, flow meter, LCD
- **Low power consumption**
  - MCU consumption:
    - 3.4 mA active mode, CoreMark®
    - 71 µA/MHz running CoreMark®
    - 0.98 µA standby mode, RTC, 256 KB RAM
    - 0.17 µA shutdown mode, wake-up on pin
  - Ultra-low power sensor controller consumption:
    - 32 µA in 2 MHz mode
    - 849 µA in 24 MHz mode
  - Radio Consumption:
    - 5.8 mA RX at 868 MHz
    - 25.8 mA TX at +14 dBm setting at 868 MHz
- **Wireless protocol support**
  - Wi-SUN
  - Mioty
  - Amazon Sidewalk
  - Wireless M-Bus
  - SimpleLink™ TI 15.4-stack (Sub-1GHz)
  - Proprietary systems
- **High performance radio**
  - –120 dBm for 2.5 kbps long-range mode
  - –110 dBm at 50 kbps, 802.15.4, 868 MHz
- **MCU peripherals**
  - Most digital peripherals can be routed to any GPIO
  - Four 32-bit or eight 16-bit general-purpose timers
  - 12-bit SAR ADC, 200 ksps, 8 channels
  - 8-bit DAC
  - Two comparators
  - Programmable current source
  - Four UART, four SPI, two I^2C, I^2S
  - Real-time clock (RTC)
  - Integrated temperature and battery monitor
  - 30 GPIOs – none SPI flash versions
  - 26 GPIOs – SPI flash versions
- **Security enablers**
  - Supports secure boot
  - Supports secure key storage and device ID
  - Arm® TrustZone® for trusted execution environment
  - AES 128- and 256-bit cryptographic accelerator
  - Public key accelerator
  - SHA2 Accelerator (full suite up to SHA-512)
  - True random number generator (TRNG)
  - Secure debug lock
  - Software anti-rollback protection
- **Operating range**
  - On-chip buck DC/DC converter
  - 1.8 V to 3.8 V single supply voltage
  - 2.3-V to 3.6-V single supply voltage (SPI flash variants)

  - -40 to +85°C or -40 to 105°C
- **Antenna options**
  - U.FL connector for external antenna
  - ANT pin for external antenna
- **On-board SPI flash**
  - 32-Mbit, only available in SPI flash versions
- **Package**
  - Dimension: 22 mm x 15 mm x 2.15 mm
  - LCC-39
  - RoHS-compliant package
- **Regulatory compliance**
  - FCC ID: 2ABRU-SG13R
  - IC: 25657-SG13R
  - CE-RED

Applications

- 868, 902 to 928 MHz ISM and SRD systems with down to 4 kHz of receive bandwidth
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor, HVAC system controller, gateway
  - Fire safety system – smoke and heat detector, fire alarm control panel (FACP)
  - Video surveillance – IP network camera
  - Elevators and escalators – elevator main control panel for elevators and escalators
- Grid infrastructure
  - Smart meters – water meter, gas meter, electricity meter, and heat cost allocators
  - Grid communications – wireless communications and long-range sensor applications
  - Other alternative energy – energy harvesting, solar inverters
- Industrial transport – asset tracking
- Factory automation and control
- Medical
- Electronic point of sale (EPOS) – Electronic Shelf Label (ESL)
- Personal electronics
  - Connected peripherals – consumer wireless module
  - Home theater & entertainment – smart speakers, set-top box
  - Gaming
  - Wearables (non-medical)

Module Family

Table 2. Module Family

Product Type & Series Name	Orderable Part Number	Chipset & Core	On-chip Flash Size (KB)	On-chip SRAM Size (KB)	Connectivity	Antenna Options	On-Board SPI Flash (Mbit)	Operating Temperature (℃)	Size (mm)
Module BDE-SG13R	BDE-SG1314R10U32	CC1314R10 Cortex-M33	1024	296	Sub-1GHz Wireless M-Bus & mioty & Wi-SUN & Sidewalk	U.FL connector	32	-40 to +85	22 X 15 X 2.15
	BDE-SG1314R10N32					ANT pin			
	BDE-SG1314R10U0					U.FL connector	0		
	BDE-SG1314R10N0					ANT pin			
	BDE-SG1314R10U32-IN					U.FL connector	32	-40 to +105	
	BDE-SG1314R10N32-IN					ANT pin			
	BDE-SG1314R10U0-IN					U.FL connector	0		
	BDE-SG1314R10N0-IN					ANT pin			
	BDE-SG1312R7U32	CC1312R7 Cortex-M4F	704	152	Sub-1GHz Wireless M-Bus & mioty & Wi-SUN & Sidewalk	U.FL connector	32	-40 to +85	
	BDE-SG1312R7N32					ANT pin			
	BDE-SG1312R7U0					U.FL connector	0		
	BDE-SG1312R7N0					ANT pin			
	BDE-SG1312R7U32-IN					U.FL connector	32	-40 to +105	
	BDE-SG1312R7N32-IN					ANT pin			
	BDE-SG1312R7U0-IN					U.FL connector	0		
	BDE-SG1312R7N0-IN					ANT pin			
	BDE-SG1312RU32	CC1312R Cortex-M4F	352	88	Sub-1GHz Wireless M-Bus & mioty & Wi-SUN & Sidewalk	U.FL connector	32	40 to +85	
	BDE-SG1312RN32					ANT pin			
	BDE-SG1312RU0					U.FL connector	0		
	BDE-SG1312RN0					ANT pin			
	BDE-SG1312RU32-IN					U.FL connector	32	-40 to +105	
	BDE-SG1312RN32-IN					ANT pin			
	BDE-SG1312RU0-IN					U.FL connector	0		
	BDE-SG1312RN0-IN					ANT pin			
	BDE-SG1311R3U32	CC1311R3 Cortex-M4	352	40	Sub-1GHz Wireless M-Bus & mioty	U.FL connector	32	-40 to +85	
	BDE-SG1311R3N32					ANT pin			
	BDE-SG1311R3U0					U.FL connector	0		
	BDE-SG1311R3N0					ANT pin			
	BDE-SG1311R3U32-IN					U.FL connector	32	-40 to +105	
	BDE-SG1311R3N32-IN					ANT pin			
	BDE-SG1311R3U0-IN					U.FL connector	0		
	BDE-SG1311R3N0-IN					ANT pin			

Naming Convention

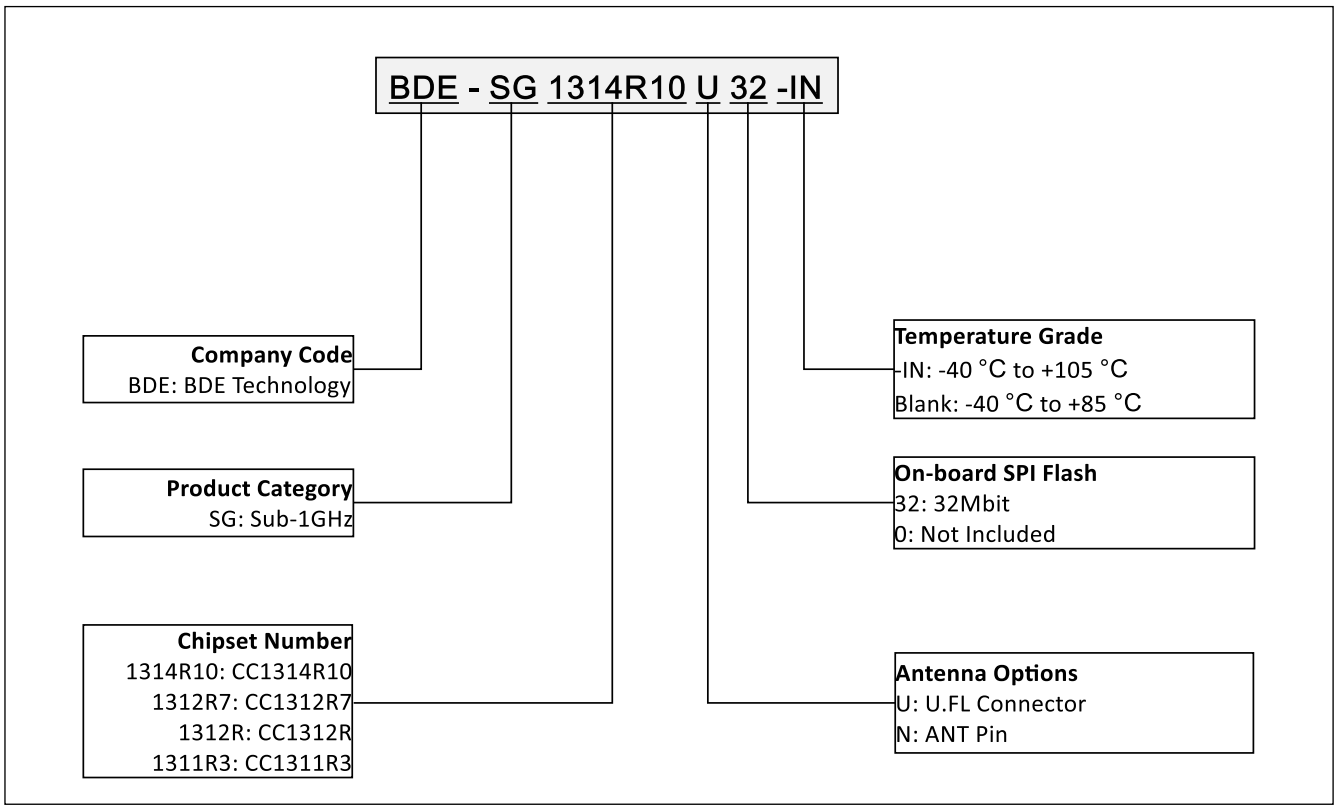

Figure 1. Module Naming Convention

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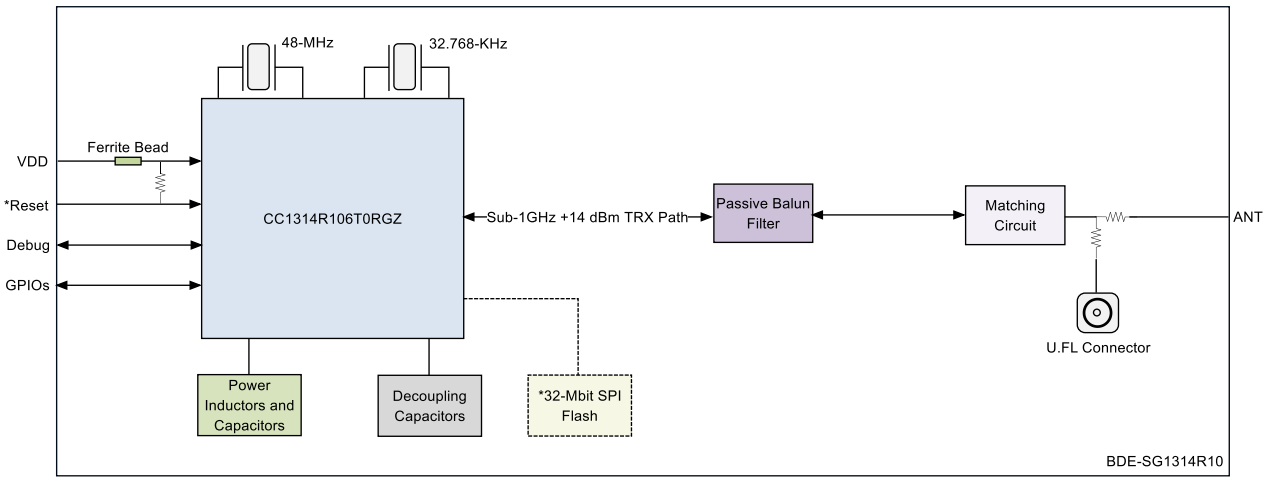
[1] CC1314R10 resources: https://www.ti.com/product/CC1314R10

1. System Overview

1.1. Block Diagram

BDE-SG1314R10 module series is based on the Texas Instruments' CC1314R10 single chip wireless MCU. The module integrates all required system-level hardware components including clocks, balun filter, other passives, and U.FL connector into a small PCB form factor.

The module, as seen in Figure 2, comprises of:
- 48-MHz XTAL
- 32.768-kHz XTAL
- Power inductors and capacitors
- Pull-up resistor
- Passive balun filter
- Decoupling capacitors
- Matching circuit
- ANT Pin (BDE-SG1314R10N variants)
- U.FL connector (BDE-SG1314R10U variants)



(1) The 32-Mbit SPI flash is only included in module BDE-SG1314R10x32 variants;
(2) Reset pin has an internal pull-up resistor and a decoupling capacitor.

Figure 2. BDE-SG1314R10 Module Block Diagram

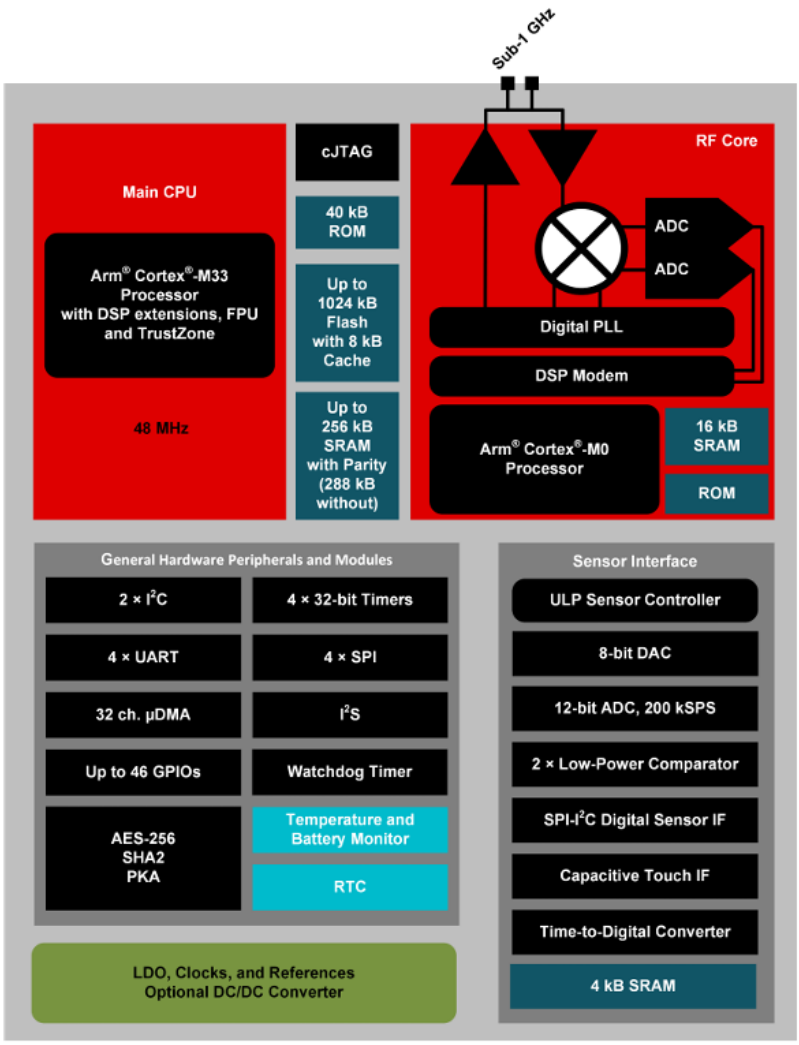


Figure 3. The Block Diagram of CC1314R10 (Adopted form CC1314R10 Datasheet)

1.2. System CPU

The BDE-SG1314R10 module series utilizes CC1314R10 SimpleLink™ Wireless MCU. The MCU contains an Arm® Cortex®-M33 system CPU with TrustZone®, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

1.3. Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

1.3.1. Proprietary Radio Formats

The BDE-SG1314R10 radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

Table 3 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

Table 3. Feature Support

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Programmable preamble, sync word and CRC	Yes	Yes	Yes	No
Programmable receive bandwidth	Yes	Yes	Yes (down to 4 kHz)	Yes
Data / Symbol rate(3)	20 to 1000 kbps	≤ 2 Msps	≤ 100 ksps	≤ 20 ksps
Modulation format	2- (G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK 4-(G)FSK	2- (G)FSK
Dual Sync Word	Yes	Yes	No	No
Carrier Sense (1) (2)	Yes	No	No	No
Preamble Detection(2)	Yes	Yes	Yes	No
Data Whitening	Yes	Yes	Yes	Yes
Digital RSSI	Yes	Yes	Yes	Yes
CRC filtering	Yes	Yes	Yes	Yes
Direct-sequence spread spectrum (DSSS)	No	No	No	1:2 1:4 1:8
Forward error correction (FEC)	No	No	No	Yes
Link Quality Indicator (LQI)	Yes	Yes	Yes	Yes

(1) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD_PROP_CS radio API;

(2) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power;

(3) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.

1.4. Memory

The up to 1024 KB nonvolatile (Flash) memory provides storage for code and data in two banks. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to eight 32 kB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. Parity can be disabled for an additional 32kB that can be allocated for general-purpose SRAM. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8 kB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4 kB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

The module series also provides an option with integrated an on-board 32-Mbit SPI flash for the applications that need to store large application data.

1.5. Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy

alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.

- The ADC is a 12-bit 200 ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs.
- Dedicated SPI master with up to 6 MHz clock speed.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

1.6. Cryptography

The device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- True Random Number Generator (TRNG) module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- Secure Hash Algorithm 2 (SHA-2) with support for SHA224, SHA256, SHA384, and SHA512.
- Advanced Encryption Standard (AES) with 128, 192 and 256 bit key lengths.
- Public Key Accelerator - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for application or stack:

- Key Agreement Schemes
- Signature Generation
- Curve Support
- Message Authentication Codes
- Block cipher mode of operation
- Hash Algorithm
- True random number generation

Other capabilities, such as RSA encryption and signatures (using keys as large as 2048 bits) as well as other ECC curves such as Curve1174, can be implemented using the provided public key accelerator but are not part of the TI SimpleLink SDK for the CC1314R10 device.

1.7. Timers

A large selection of timers are available as part of the device. These timers are:

- Real-Time Clock (RTC)
- General Purpose Timers (GPTIMER)
- Sensor Controller Timers

- Radio Timer
- Watchdog timer
- Always On Watchdog Timer (AON_WDT)

1.8. Serial Peripherals and I/O

The SPI interface provides a standardized synchronous serial interface to communicate with devices compatible with SPI (3 and 4 wire), MICROWIRE and TI Synchronous Serial Format. The SPIs support master/slave operation up to 12 MHz, programmable clock bit rate with prescaler, as well as configurable phase and polarity.

The UART interface implements universal asynchronous receiver and transmitter functions. The UART supports flexible baud-rate generation up to a maximum of 3 Mbps with FIFO, multiple data sizes, stop and parity bits as well as hardware handshake.

The I2S interface provides a standardized interface to exchange digital audio with devices compatible with this standard, including ADCs, DACs and CODECs. The I2S can also receive pulse-density modulation (PDM) data from devices such as digital microphones and perform conversion to PCM data.

The I2C interface enables low speed serial communications with devices compatible with the I2C standard. The I2C interface can handle both standard (100 kHz) and fast (400 kHz) speeds, as well as four modes of operation: master transmit/receive and slave transmit/receive.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in bold in Section 2.1. All digital peripherals can be connected to any digital pin on the device.

1.9. Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

1.10. µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

1.11. Debug

The debug subsystem implements two IEEE standards for debug and test purposes:

IEEE 1149.7 Class 4: Reduced-pin and Enhanced-functionality Test Access Port and Boundary-scan Architecture. This is known by the acronym cJTAG (compact JTAG) and this device uses only two pins to communicate to the target: TMS (JTAG_TMSC) and TCK (JTAG_TCKC). This is the default mode of operation.

IEEE standard 1149.1: Test Access Port and Boundary Scan Architecture Test Access Port (TAP). This standard is known by the acronym JTAG and this device uses four pins to communicate to the target: TMS (JTAG_TMSC), TCK (JTAG_TCKC), TDI (JTAG_TDI) and TDO (JTAG_TDO).

The debug subsystem also implements a user-configurable firewall to control unauthorized access to debug/test ports.

1.12. Clock Systems

The module has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

The module includes two crystals on board, a high frequency crystal (HFXT) with 48-MHz and a low frequency crystal (LFXT) with 32.768-KHz.

1.13. Network Processor

Depending on the product configuration, the device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

1.14. Power Management

To minimize power consumption, the BDE-SG1314R10 series supports a number of power modes and power management features (see Table 4).

Table 4. Power Modes

Mode	Software Configurable Power Modes				Reset Pin Held
	Active	Idle	Standby	Shutdown	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off
Always-on Watchdog timer (AON_WDT)	Available	Available	Available	Off	Off

In Active mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 4).

In Idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In Standby mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In Shutdown mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a wake from shutdown pin wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently

of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

The power, RF and clock management for the CC1314R10 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1314R10 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples is offered free of charge in source code.

1.15. Antenna

The module series provides two options for connecting external antenna, integrated U.FL connector and ANT pin. Refer to Section 7.1.1 for certified antenna list.

2. Pinout Functions

The module series is with LCC-39 package, 39 pads are exposed for user. This section describes pinout functions of the module in details.

2.1. Pin Diagram

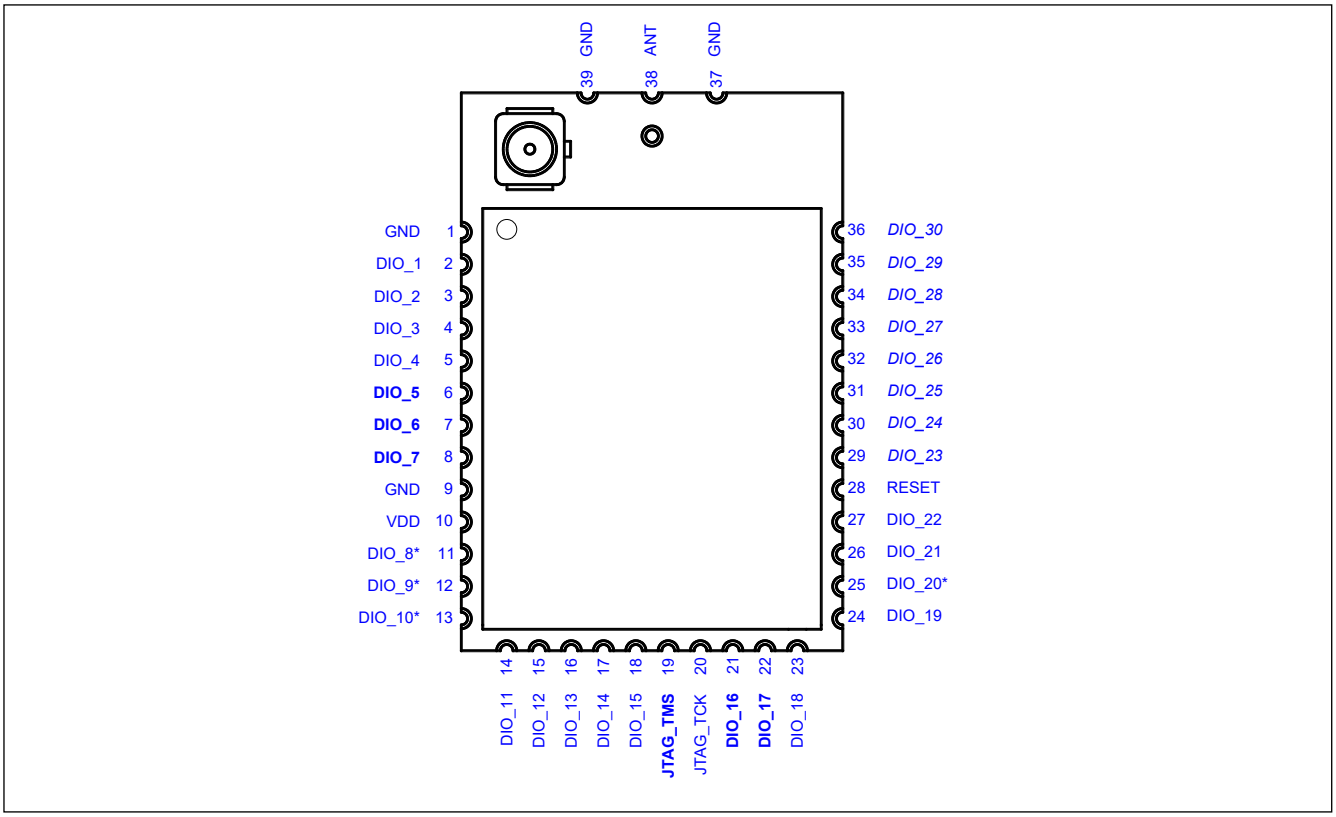


Figure 4. Pin Diagram of BDE-SG1314R10 (Top View)

The following I/O pins marked in **bold** in Figure 4 have high-drive capabilities:

- Pin 6, DIO_5
- Pin 7, DIO_6
- Pin 8, DIO_7
- Pin 19, JTAG_TMSC
- Pin 21, DIO_16
- Pin 22, DIO_17

The following I/O pins marked in *italics* in Figure 4 have analog capabilities:

- Pin 29, DIO_23
- Pin 30, DIO_24
- Pin 31, DIO_25
- Pin 32, DIO_26
- Pin 33, DIO_27
- Pin 34, DIO_28
- Pin 35, DIO_29

- Pin 36, DIO_30

The following four I/O pins are assigned to on-board 32-Mbit SPI flash for SPI flash variants:

- Pin 11, SFL_MISO_DIO_8
- Pin 12, SFL_MOSI_DIO_9
- Pin 13, SFL_CLK_DIO_10
- Pin 25, SFL_CS_DIO_20

2.2. Pin Attributes and Pin Multiplexing

Table 5 describes the definitions of the pins of the module.

Table 5. Pinout Description

Module Pin #	Pin Name	Type	CC1314R106T0RGZ Pin #	Description
1	GND	Ground	-	Power ground
2	DIO_1	I/O	6	GPIO, Sensor Controller
3	DIO_2	I/O	7	GPIO, Sensor Controller
4	DIO_3	I/O	8	GPIO, Sensor Controller
5	DIO_4	I/O	9	GPIO, Sensor Controller
6	DIO_5	I/O	10	GPIO, Sensor Controller, high-drive capability
7	DIO_6	I/O	11	GPIO, Sensor Controller, high-drive capability
8	DIO_7	I/O	12	GPIO, Sensor Controller, high-drive capability
9	GND	Ground	-	Power ground
10	VDD	Power	-	Power supply
11	DIO_8 (2)	I/O	14	GPIO, assigned as SPI_MISO of on-module SPI flash for SPI flash variants
12	DIO_9 (2)	I/O	15	GPIO, assigned as SPI_MOSI of on-module SPI flash for SPI flash variants
13	DIO_10 (2)	I/O	16	GPIO, assigned as SPI_SCLK of on-module SPI flash for SPI flash variants
14	DIO_11	I/O	17	GPIO
15	DIO_12	I/O	18	GPIO
16	DIO_13	I/O	19	GPIO
17	DIO_14	I/O	20	GPIO
18	DIO_15	I/O	21	GPIO
19	JTAG_TMS	I/O	24	JTAG TMSC, high-drive capability
20	JTAG_TCK	I	25	JTAG TCKC
21	DIO_16	I/O	26	GPIO, JTAG_TDO, high-drive capability
22	DIO_17	I/O	27	GPIO, JTAG_TDI, high-drive capability
23	DIO_18	I/O	28	GPIO
24	DIO_19	I/O	29	GPIO
25	DIO_20 (2)	I/O	30	GPIO, assigned as SPI_CS of on-module SPI flash for SPI flash variants
26	DIO_21	I/O	31	GPIO
27	DIO_22	I/O	32	GPIO
28	RESET	I	35	Reset, active-low, 100K ohm internal pull-up resistor

Module Pin #	Pin Name	Type	CC1314R106T0RGZ Pin #	Description
29	DIO_23	I/O	36	GPIO, Sensor Controller, analog capability
30	DIO_24	I/O	37	GPIO, Sensor Controller, analog capability
31	DIO_25	I/O	38	GPIO, Sensor Controller, analog capability
32	DIO_26	I/O	39	GPIO, Sensor Controller, analog capability
33	DIO_27	I/O	40	GPIO, Sensor Controller, analog capability
34	DIO_28	I/O	41	GPIO, Sensor Controller, analog capability
35	DIO_29	I/O	42	GPIO, Sensor Controller, analog capability
36	DIO_30	I/O	43	GPIO, Sensor Controller, analog capability
37	GND	Ground	-	Power ground
38	ANT	RF	-	Antenna port for -N variants
	NC	-	-	No connect for -U variants
39	GND	Ground	-	Power ground

(1) For pin multiplexing details, refer to CC1314R10 SimpleLink™ Arm® Cortex®-M33 Sub-1GHz wireless MCU with 1MB flash and up to 296KB SRAM;
(2) These four pins are assigned as SPI for on-board 32-Mbit flash in SPI flash variants modules and are not exposed for user, leave floating;
(3) For operating voltage, please refer to Table 9.

2.3. Connections for Unused Pins

Table 6. Connections for Unused Pins

Function	Signal Name	Acceptable Practice	Preffered Practice
GPIO (Digital or analog)	DIOn	NC or GND	NC

3. Specifications

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Over operating free-air temperature range (unless otherwise noted).

Table 7. Absolute Maximum Ratings

Parameter	MIN	MAX	Unit	Notes
VDD	-0.3	4.1	V	
Voltage on any digital pins	-0.3	VDD+0.3≤4.1	V	
Voltage on ADC input	-0.3	VDD	V	Voltage scaling enabled
	-0.3	1.49	V	Voltage scaling disabled, internal reference
	-0.3	VDD/2.9	V	Voltage scaling disabled, VDD as reference
Storage temperature	-40	125	°C	

3.1.2. ESD Ratings

Table 8. ESD Ratings

Parameter	Description	Value	Unit	Note
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

3.1.3. Recommended Operating Conditions

Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.

Over operating free-air temperature range (unless otherwise noted).

Table 9. Recommended Operating Conditions

Parameter	MIN	TYP	MAX	Unit
VDD	1.8	3.3	3.8	V
VDD (For SPI flash variants)	2.3	3.3	3.8	V
Operating temperature	-40	-	85	°C
Operating temperature (-IN variants)	-40	-	105	°C
Rising supply voltage slew rate	0		100	mV/us
Falling supply voltage slew rate	0		20	mV/us

3.1.4. Power Consumption

The measurement is made with T_A = 25 °C, VDD = 3.3 V, DCDC enabled, GLDO disabled, unless otherwise noted.

Table 10. Power Consumption – Power Modes

Power Mode	Test Condition	TYP	Unit
Reset	Reset. RESET pin asserted or VDD below power-on-reset threshold	150	nA
Shutdown	Shutdown. No clocks running, no retention	171	nA
Standby without cache retention	RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	0.98	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	0.88	uA
	RTC running, CPU, 256 kB RAM and (partial) register retention. XOSC_LF	1.08	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. XOSC_LF	0.99	uA
Standby with cache retention	RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	2.24	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	2.16	uA
	RTC running, CPU, 256 kB RAM and (partial) register retention. XOSC_LF	2.34	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. XOSC_LF	2.25	uA
Idle	Supply Systems and RAM powered RCOSC_HF	635	uA
Active	MCU running CoreMark at 48 MHz with parity enabled RCOSC_HF	3.5	mA
	MCU running CoreMark at 48 MHz with parity disabled RCOSC_HF	3.4	mA
Peripheral, power domain	Delta current with domain enabled	62.4	uA
Peripheral, Serial power domain	Delta current with domain enabled	5.83	uA
Peripheral, RF Core	Delta current with power domain enabled, clock enabled, RF core idle	102.0	uA
Peripheral, µDMA	Delta current with clock enabled, module is idle	58.0	uA
Peripheral, Timers	Delta current with clock enabled, module is idle	97.2	uA
Peripheral, I2C	Delta current with clock enabled, module is idle	9.8	uA
Peripheral, I2S	Delta current with clock enabled, module is idle	22.2	uA
Peripheral, SPI	Delta current with clock enabled, module is idle	55.8	uA
Peripheral, UART	Delta current with clock enabled, module is idle	114.2	uA
Peripheral, CRYPTO (AES)	Delta current with clock enabled, module is idle	15.5	uA
Peripheral, PKA	Delta current with clock enabled, module is idle	66.6	uA
Peripheral, TRNG	Delta current with clock enabled, module is idle	21.0	uA
Sensor Controller Engine, Active	24 MHz, infinite loop	849.0	uA
Sensor Controller Engine, Low-power	2 MHz, infinite loop	32.0	uA

Table 11. Power Consumption – Radio Modes

Power Mode	Test Condition	TYP	Unit
Radio receive current	868 MHz	5.8	mA
Radio transmit current	0 dBm output power setting 868 MHz	9.5	mA
	+10 dBm output power setting 868 MHz	14.1	mA
	+14 dBm output power setting 868 MHz	25.8	mA

3.1.5. Clock Characteristics

Table 12. 48-MHz Crystal Oscillator (XOSC_HF) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			48		MHz
ESR, Equivalent series resistance				40	Ω
Frequency tolerance	TA: 25°C	-10		10	ppm
Frequency stability	TA: -40°C ~ 85°C	-20		20	ppm
CL, Crystal load capacitance			7		pF

Table 13. 32.768-KHz Crystal Oscillator (XOSC_LF) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32.768		KHz
ESR, Equivalent series resistance				70	kΩ
Frequency tolerance	TA: 25°C	-20		20	ppm
CL, Crystal load capacitance			12.5		pF

3.1.6. Reset Timing

Table 14. Reset Timing

Parameter	MIN	TYP	MAX	Unit
nRESET low duration	1			us

3.1.7. UART Characteristics

Table 15. UART Characteristics

Parameter	MIN	TYP	MAX	Unit
UART baud rate			3	MBaud

3.1.8. SPI Characteristics

Table 16. SPI Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
SPI clock frequency	Primary Mode 1.71 < VDD < 3.8			12	MHz
	Secondary Mode 2.7 < VDD < 3.8			8	
	Secondary Mode VDD < 2.7			7	
SPI duty cycle		45	50	55	%

For SPI characteristics or other details, please refer to CC1314R10 datasheet: CC1314R10 SimpleLink™ Arm® Cortex®-M33 Sub-1GHz wireless MCU with 1MB flash and up to 296KB SRAM

3.1.9. GPIO DC Characteristics

Table 17. GPIO DC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
T_A = 25 °C, V_{DD} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DD} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V
T_A = 25 °C, V_{DD} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a High	0.8*VDD			V
VIL	Highest GPIO input voltage reliably interpreted as a Low			0.2*VDD	V

3.1.10. ADC Characteristics

Table 18. ADC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Resolution			12		Bits
Sample Rate				200	ksps
Offset	Internal 4.3V equivalent reference		-0.24		LSB
Gain error	Internal 4.3V equivalent reference		7.14		LSB

Parameter	Test Condition	MIN	TYP	MAX	Unit
Differential nonlinearity			> -1		LSB
Integral nonlinearity			± 4		LSB
Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3		V
Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: Vref = 4.3 V × 1408 / 4095		1.48		V
Reference voltage	VDD as reference, input voltage scaling enabled		VDD		V
	VDD as reference, input voltage scaling disabled		VDD/2.82		V
Input Impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		> 1		MΩ

For ADC characteristics or other details, please refer to CC1314R10 datasheet: CC1314R10 SimpleLink™ Arm® Cortex®-M33 Sub-1GHz wireless MCU with 1MB flash and up to 296KB SRAM

3.1.11. DAC Characteristics

Table 19. DAC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Resolution			8		Bits
Supply voltage	Any load, any VREF, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
	External Load, any VREF, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	V
	Any load, VREF = DCOUPL, pre-charge ON	2.6		3.8	V
Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
	Buffer OFF (internal load)	16		1000	kHz

For DAC characteristics or other details, please refer to CC1314R10 datasheet: CC1314R10 SimpleLink™ Arm® Cortex®-M33 Sub-1GHz wireless MCU with 1MB flash and up to 296KB SRAM

3.1.12. Comparator Characteristics

Table 20. Low-Power Clocked Comparator Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Clock frequency			32		KHz
Internal reference voltage	Using internal DAC with VDDS as reference voltage, DAC code = 0 - 255	0.024		2.865	V
Offset	Measured at VDDS / 2, includes error from internal DAC		±5		mV
Decision time	Step from –50 mV to 50 mV		1		Clock Cycle

Table 21. Continuous Time Comparator Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Offset	Measured at VDD/2		± 5		mV
Decision time	Step from -10 mV to 10 mV		0.78		us
Current consumption	Internal reference		8.6		uA

3.2. RF Characteristics

The measurement is made with the evaluation board for BDE-SG1314R10 with T_A = 25 °C, VDD = 3.3 V, DCDC enabled, GLDO disabled, unless otherwise noted.

3.2.1. 861 MHz to 1054 MHz Performance: Receiver Characteristics

Table 22. 861 MHz to 1054 MHz Performance: Receiver Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
General Parameters					
Digital channel filter programmable receive bandwidth		4		4000	kHz
Data rate step size			1.5		bps
Spurious emissions 25 MHz to 1 GHz	868 MHz		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		
Wi-SUN, 50 kbps, ± 12.5 kHz deviation, 2-GFSK, 78 kHz RX BW, #1a					
Sensitivity	MRFSK, 866.6MHz, 10% PER, 250 byte payload		-105		dBm
Saturation limit	10% PER, 250 byte payload, 866.6MHz		10		
Selectivity, +100 kHz	10% PER, 250 byte payload, 866.6MHz. Wanted signal 3 dB above sensitivity level.		33		dB
Selectivity, -100 kHz			31		
Selectivity, +200 kHz			38		
Selectivity, -200 kHz			37		

Parameter	Test Condition	MIN	TYP	MAX	Unit
RSSI dynamic range	Starting from the sensitivity limit		93		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 50 kbps, ± 25 kHz deviation, 2-GFSK, 100 kHz RX BW, #1b					
Sensitivity	MRFSK, 918.2MHz, 10% PER, 250 byte payload		-106		dBm
Saturation limit	10% PER, 250 byte payload, 918.2MHz		10		
Selectivity, +200 kHz	10% PER, 250 byte payload, 918.2MHz. Wanted signal 3 dB above sensitivity level.		37		dB
Selectivity, -200 kHz			35		
Selectivity, +400 kHz			42		
Selectivity, -400 kHz			41		
RSSI dynamic range	Starting from the sensitivity limit		95		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 100 kbps, ± 25 kHz deviation, 2-GFSK, 135 kHz RX BW, #2a					
Sensitivity	MRFSK, 866.6MHz, 10% PER, 250 byte payload		-105		dBm
Saturation limit	10% PER, 250 byte payload, 866.6MHz		10		
Selectivity, +200 kHz	10% PER, 250 byte payload, 866.6MHz. Wanted signal 3 dB above sensitivity level.		40		dB
Selectivity, -200 kHz			38		
Selectivity, +400 kHz			46		
Selectivity, -400 kHz			44		
RSSI dynamic range	Starting from the sensitivity limit		95		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 100 kbps, ± 50 kHz deviation, 2-GFSK, 208 kHz RX BW, #2b					
Sensitivity	MRFSK, 920.9MHz, 10% PER, 250 byte payload		-102		dBm
Saturation limit	10% PER, 250 byte payload, 920.9MHz		10		
Selectivity, +400 kHz	10% PER, 250 byte payload, 920.9MHz. Wanted signal 3 dB above sensitivity level.		42		dB
Selectivity, -400 kHz			39		
Selectivity, +800 kHz			52		
Selectivity, -800 kHz			46		
RSSI dynamic range	Starting from the sensitivity limit		91		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 150 kbps, ± 37.5 kHz deviation, 2-GFSK, 273 kHz RX BW, #3					
Sensitivity	MRFSK, 918.4MHz, 10% PER, 250 byte payload		-99		dBm
Saturation limit	10% PER, 250 byte payload, 918.4MHz		10		
Selectivity, +400 kHz	10% PER, 250 byte payload, 918.4MHz. Wanted signal 3 dB above sensitivity level.		41		dB
Selectivity, -400 kHz			39		
Selectivity, +800 kHz			50		
Selectivity, -800 kHz			46		
RSSI dynamic range	Starting from the sensitivity limit		86		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 200 kbps, ± 50 kHz deviation, 2-GFSK, 335 kHz RX BW, #4a					
Sensitivity	MRFSK, 918.4MHz, 10% PER, 250 byte payload		-99		dBm
Saturation limit	10% PER, 250 byte payload, 918.4MHz		10		
Selectivity, +400 kHz	10% PER, 250 byte payload, 918.4MHz. Wanted signal 3 dB above sensitivity level.		42		dB
Selectivity, -400 kHz			40		

Parameter	Test Condition	MIN	TYP	MAX	Unit
Selectivity, +800 kHz			51		
Selectivity, -800 kHz			47		
RSSI dynamic range	Starting from the sensitivity limit		91		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 200 kbps, ± 100 kHz deviation, 2-GFSK, 416 kHz RX BW, #4b					
Sensitivity	MRFSK, 920.8MHz, 10% PER, 250 byte payload		-98		dBm
Saturation limit	10% PER, 250 byte payload, 920.8MHz		10		
Selectivity, +600 kHz	10% PER, 250 byte payload, 920.8MHz. Wanted signal 3 dB above sensitivity level.		46		dB
Selectivity, -600 kHz			43		
Selectivity, +1200 kHz			54		
Selectivity, -1200 kHz			51		
RSSI dynamic range	Starting from the sensitivity limit		86		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
Wi-SUN, 300 kbps, ± 75 kHz deviation, 2-GFSK, 496 kHz RX BW, #5					
Sensitivity	MRFSK, 917.6MHz, 10% PER, 250 byte payload		-97		dBm
Saturation limit	10% PER, 250 byte payload, 917.6MHz		10		
Selectivity, +600 kHz	10% PER, 250 byte payload, 917.6MHz. Wanted signal 3 dB above sensitivity level.		42		dB
Selectivity, -600 kHz			37		
Selectivity, +1200 kHz			51		
Selectivity, -1200 kHz			40		
RSSI dynamic range	Starting from the sensitivity limit		86		
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		
802.15.4-2020, 10 kbps, 2-FSK, 26 kHz RX BW, Mode #1a					
Sensitivity	FSK, 915.0MHz, 20 byte PSDU < 10% PER		-111		dBm
Sensitivity	FSK, 868.3MHz, 20 byte PSDU < 10% PER		-111		
Saturation limit	PSDU length 20 octets; PER < 10%, 868.3MHz		10		
Selectivity, +50 kHz	PSDU length 20 octets; PER < 10%, 868.3MHz		36		dB
Selectivity, -50 kHz			36		
Selectivity, +100 kHz			40		
Selectivity, -100 kHz			39		
Selectivity, +200 kHz			44		
Selectivity, -200 kHz			37		
Blocking, +1 MHz			60		
Blocking, -1 MHz			59		
Blocking, +2 MHz			64		
Blocking, -2 MHz			64		
Blocking, +5 MHz			75		
Blocking, -5 MHz			74		
Blocking, +10 MHz			79		
Blocking, -10 MHz			79		
Blocking + 5% Fc. (45.75 MHz)	10% PER, 20 byte payload, 866.6 MHz 802.15.4g mandatory mode, wanted signal -94 dBm. 3 dB above usable sensitivity limit usable sensitivity -97 dBm.		-15		dBm
Blocking - 5% Fc. (-45.75 MHz)			-15		dBm

Parameter	Test Condition	MIN	TYP	MAX	Unit
Image rejection (image compensation enabled)	PSDU length 20 octets; PER < 10%, 866.6MHz. Wanted signal 3dB above sensitivity limit.		39		dB
Image rejection (image compensation enabled)	PSDU length 20 octets; PER < 10%, 866.6MHz		39		dB
RSSI dynamic range	Starting from the sensitivity limit		100		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Negative offset		-12		ppm
Frequency error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Positive offset		12		ppm
Symbol rate error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Negative offset		-1000		ppm
Symbol rate error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Positive offset		1000		ppm
802.15.4-2020, 20 kbps, 2-FSK, 52 kHz RX BW, Mode #1b					
Sensitivity	FSK, 20 kbps, ±10 kHz deviation, 2-GFSK, 915.0MHz, 52 kHz RX BW, 20 byte PSDU < 10% PER		-107		dBm
Sensitivity	FSK, 20 kbps, ±10 kHz deviation, 2-GFSK, 868.3MHz, 52 kHz RX BW, 20 byte PSDU < 10% PER		-109		dBm
Saturation limit	PSDU length 20 octets; PER < 10%, 868.3MHz		10		dBm
Selectivity, +100 kHz	20 byte PSDU < 10% PER, 868.3MHz		38		dB
Selectivity, -100 kHz			36		
Selectivity, +200 kHz			44		
Selectivity, -200 kHz			42		
Selectivity, +400 kHz			49		
Selectivity, -400 kHz			44		
Blocking, +1 MHz			58		
Blocking, -1 MHz			54		
Blocking, +2 MHz			61		
Blocking, -2 MHz			61		
Blocking, +5 MHz			70		
Blocking, -5 MHz			70		
Blocking, +10 MHz			75		
Blocking, -10 MHz			76		
Blocking + 5% Fc. (45.75 MHz)	20 byte PSDU < 10% PER, 866.6 MHz, wanted signal -94 dBm. 3 dB above usable sensitivity limit according to usable sensitivity -97 dBm.		-13		dBm
Blocking - 5% Fc. (-45.75 MHz)			-13		dBm
Image rejection (image compensation enabled)	20 byte PSDU < 10% PER, 866.6MHz, Wanted signal 3 dB above sensitivity level		39		dB
Image rejection (image compensation enabled)	20 byte PSDU < 10% PER, 866.6MHz		39		dB
RSSI dynamic range	Starting from the sensitivity limit		100		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB

Parameter	Test Condition	MIN	TYP	MAX	Unit
Frequency error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Negative offset		24		ppm
Frequency error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Positive offset		24		ppm
Symbol rate error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Negative offset		-1000		ppm
Symbol rate error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Positive offset		1000		ppm
802.15.4-2020, 200 kbps, ± 50 kHz deviation, 2-GFSK, 311 kHz RX BW					
Sensitivity	BER = 10^{-2}, 868MHz		-101		dBm
Sensitivity	BER = 10^{-2}, 915MHz		-100		
Selectivity, +400 kHz	BER = 10^{-2}, 915MHz. Wanted signal 3 dB above sensitivity limit.		45		dB
Selectivity, -400 kHz			45		
Selectivity, +800 kHz			52		
Selectivity, -800 kHz			47		
Blocking, +2 MHz			59		
Blocking, -2 MHz			56		
Blocking, +10 MHz			71		
Blocking, -10 MHz			70		
802.15.4-2020, 500 kbps, ± 190 kHz deviation, 2-GFSK, 622 kHz RX BW					
Sensitivity 500 kbps	915 MHz, 1% PER, 127 byte payload		-94.5		dBm
Selectivity, ± 1 MHz	915 MHz, 1% PER, 127 byte payload. Wanted signal at -88 dBm		34		dB
Selectivity, ± 2 MHz	915 MHz, 1% PER, 127 byte payload. Wanted signal at -88 dBm		46		dB
Co-channel rejection	915 MHz, 1% PER, 127 byte payload. Wanted signal at -71 dBm		-8		dB
SimpleLink™ Long Range 2.5/5 kbps (20 ksps), ±5 kHz Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = 10^{-2}, 868MHz		-120		dBm
Sensitivity	2.5 kbps, BER = 10^{-2}, 915MHz		-120		dBm
Sensitivity	5 kbps, BER = 10^{-2}, 868MHz		-118		dBm
Sensitivity	5 kbps, BER = 10^{-2}, 915MHz		-118		dBm
Saturation limit	2.5 kbps, BER = 10^{-2}, 868MHz		10		dBm
Selectivity, +100 kHz	2.5 kbps, BER = 10^{-2}, 868MHz		49		dB
Selectivity, -100 kHz			49		
Selectivity, +200 kHz			52		
Selectivity, -200 kHz			48		
Selectivity, +300 kHz			54		
Selectivity, -300 kHz			48		
Blocking, +1 MHz	2.5 kbps, BER = 10^{-2}, 868MHz		65		dB
Blocking, -1 MHz			60		
Blocking, +2 MHz			70		
Blocking, -2 MHz			68		
Blocking, +5 MHz			78		
Blocking, -5 MHz			77		
Blocking, +10 MHz			87		
Blocking, -10 MHz			92		

Parameter	Test Condition	MIN	TYP	MAX	Unit
Image rejection (image compensation enabled)	2.5 kbps, BER = 10^{-2}, 868MHz		47		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error tolerance (ppm)	2.5 kbps, measured at -110 dBm		-24/26		ppm
Symbol rate error tolerance (ppm)	2.5 kbps, measured at -110 dBm		-90/70		ppm
Narrowband, 9.6 kbps ± 2.4 kHz deviation, 2-GFSK, 868 MHz, 17.1 kHz RX BW					
Sensitivity	1% BER		-118		dBm
Adjacent Channel Rejection	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6dBm). Interferer ± 20 kHz		42		dB
Alternate Channel Rejection	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6dBm). Interferer ± 40 kHz		42		dB
Blocking, ± 1 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6dBm).		66		dB
Blocking, ± 2 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6dBm).		71		dB
Blocking, ± 10 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6dBm).		85		dB
802.15.4, 50 kbps, ±25 kHz Deviation, 2-GFSK, 100 kHz RX BW (Legacy)					
Sensitivity	BER = 10^{-2}, 868MHz		-110		dBm
Sensitivity	BER = 10^{-2}, 915MHz		-109		
Saturation limit	BER = 10^{-2}, 868MHz		10		
Selectivity, +200 kHz	BER = 10^{-2}, 868MHz		44		dB
Selectivity, -200 kHz			44		
Selectivity, +400 kHz			54		
Selectivity, -400 kHz			44		
Blocking, +1 MHz			57		
Blocking, -1 MHz			57		
Blocking, +2 MHz			61		
Blocking, -2 MHz			61		
Blocking, +5 MHz			67		
Blocking, -5 MHz			67		
Blocking, +10 MHz			76		
Blocking, -10 MHz			76		
Blocking + 5% Fc. (43.42 MHz)	BER = 10^{-2}, 868MHz 802.15.4g mandatory mode, wanted signal -94 dBm. 3 dB above usable sensitivity limit usable sensitivity -97 dBm.		-15		dBm
Blocking - 5% Fc. (-43.42 MHz)			-15		dBm
Image rejection (image compensation enabled)	BER = 10^{-2}, 868MHz. Wanted signal 3 dB above sensitivity limit		39		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error	1% BER, measured at -100 dBm (10 dB above sensitivity level).		-30		ppm

Parameter	Test Condition	MIN	TYP	MAX	Unit
tolerance (ppm)	Negative offset				
Frequency error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Positive offset		25		ppm
Symbol rate error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Negative offset		-2000		ppm
Symbol rate error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Positive offset		2000		ppm
802.15.4, 100 kbps, ±25 kHz Deviation, 2-GFSK, 137 kHz RX BW					
Sensitivity 100 kbps	868 MHz, 1% PER, 127 byte payload		-104		dBm
Selectivity, ±200 kHz	868 MHz, 1% PER, 127 byte payload. Wanted signal at -96 dBm		38		dB
Selectivity, ±400 kHz			44		
Co-channel rejection	868 MHz, 1% PER, 127 byte payload. Wanted signal at -79 dBm		-9		
Generic OOK (16.384 kbps, OOK w / Manchester encoding, 100 kHz RX BW)					
Sensitivity	OOK, 915.0 MHz, 1% PER		-108		dBm
Sensitivity	OOK, 868.8 MHz, 1% PER		-108		dBm
Saturation limit	868.3 MHz		0		dBm
Selectivity, +200 kHz	868.3 MHz. Wanted signal 3 dB above sensitivity level.		52		dB
Selectivity, -200 kHz			47		
Selectivity, +400 kHz			42		
Selectivity, -400 kHz			42		
Blocking, +1 MHz			68		
Blocking, -1 MHz			64		
Blocking, +2 MHz			68		
Blocking, -2 MHz			64		
Blocking, +5 MHz			74		
Blocking, -5 MHz			73		
Blocking, +10 MHz			68		
Blocking, -10 MHz			64		
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error tolerance (ppm)	Measured at 10 dB above sensitivity level. Negative offset		-40		ppm
Frequency error tolerance (ppm)	Measured at 10 dB above sensitivity level. Positive offset		40		ppm
Symbol rate error tolerance (ppm)	Measured at 10 dB above sensitivity level. Negative offset		-2000		ppm
Symbol rate error tolerance (ppm)	Measured at 10 dB above sensitivity level. Positive offset		2000		ppm
WB-DSSS, 240/120/60/30 kbps (480 ksym/s, 2-GFSK, ±25 kHz Deviation, FEC(Half Rate), DSSS = 1/2/4/8, 622 kHz RX BW)					
Sensitivity	240 kbps, DSSS = 1, BER = 10^{-2}, 915.0 MHz		-102		dBm
Sensitivity	120 kbps, DSSS = 2, BER = 10^{-2}, 915.0 MHz		-108		dBm
Sensitivity	60 kbps, DSSS = 4, BER = 10^{-2}, 915.0 MHz		-110		dBm
Sensitivity	30 kbps, DSSS = 8, BER = 10^{-2}, 915.0 MHz		-110		dBm
Saturation limit	915.0 MHz		0		dBm

Parameter	Test Condition	MIN	TYP	MAX	Unit
Blocking +1 MHz	240 kbps, DSSS = 1		54		dB
	120 kbps, DSSS = 2		57		
	600 kbps, DSSS = 4		57		
	30 kbps, DSSS = 8		57		
Blocking -1 MHz	240 kbps, DSSS = 1		49		
	120 kbps, DSSS = 2		50		
	600 kbps, DSSS = 4		52		
	30 kbps, DSSS = 8		53		
Blocking +2 MHz	240 kbps, DSSS = 1		54		dB
	120 kbps, DSSS = 2		55		
	600 kbps, DSSS = 4		57		
	30 kbps, DSSS = 8		58		
Blocking -2 MHz	240 kbps, DSSS = 1		53		
	120 kbps, DSSS = 2		54		
	600 kbps, DSSS = 4		56		
	30 kbps, DSSS = 8		56		
Blocking +5 MHz	240 kbps, DSSS = 1		55		dB
	120 kbps, DSSS = 2		56		
	600 kbps, DSSS = 4		58		
	30 kbps, DSSS = 8		59		
Blocking -5 MHz	240 kbps, DSSS = 1		54		
	120 kbps, DSSS = 2		55		
	600 kbps, DSSS = 4		57		
	30 kbps, DSSS = 8		58		
Blocking +10 MHz	240 kbps, DSSS = 1		69		dB
	120 kbps, DSSS = 2		70		
	600 kbps, DSSS = 4		72		
	30 kbps, DSSS = 8		73		
Blocking -10 MHz	240 kbps, DSSS = 1		65		
	120 kbps, DSSS = 2		67		
	600 kbps, DSSS = 4		69		
	30 kbps, DSSS = 8		70		
RSSI dynamic range	Starting from the sensitivity limit		85		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB

3.2.2. 861 MHz to 1054 MHz Performance: Transmitter Characteristics

Table 23. 861 MHz to 1054 MHz Performance: Transmitter Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Max output power 14dBm setting, boost mode	Minimum supply voltage (VDD) for boost mode is 2.1V, 868 MHz and 915 MHz		14.1		dBm
12dBm setting	868MHz and 915MHz		11.1		dBm
11dBm setting	868MHz and 915MHz		10.2		dBm
10dBm setting	868MHz and 915MHz		9.2		dBm

Parameter	Test Condition	MIN	TYP	MAX	Unit
9dBm setting	868MHz and 915MHz		8.2		dBm
8dBm setting	868MHz and 915MHz		7.1		dBm
7dBm setting	868MHz and 915MHz		6.3		dBm
6dBm setting	868MHz and 915MHz		5.0		dBm
5dBm setting	868MHz and 915MHz		4.0		dBm
4dBm setting	868MHz and 915MHz		3.7		dBm
3dBm setting	868MHz and 915MHz		3.3		dBm
2dBm setting	868MHz and 915MHz		2.3		dBm
1dBm setting	868MHz and 915MHz		1.0		dBm
0dBm setting	868MHz and 915MHz		0		dBm
Output power programmable range	868 MHz and 915 MHz, 1dB step size.		34		dB
Output power variation over temperature	+10 dBm setting Over recommended temperature operating range		± 2		dB
Output power variation over temperature Boost mode	+14 dBm setting Over recommended temperature operating range		± 1.5		dB

3.3. Antenna Characteristics

Refer to Section 7.1.1 for certified antenna list.

4. Mechanical Specifications

4.1. Dimensions

The following pages include mechanical, footprint drawings, and marking information.

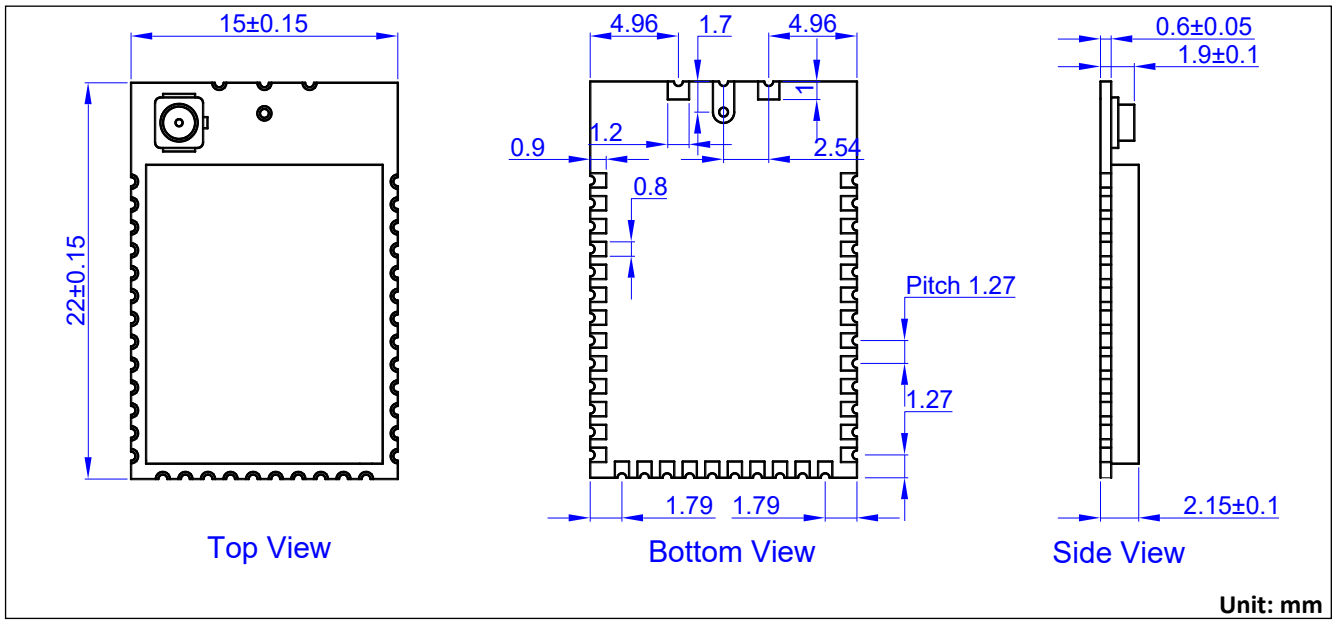


Figure 5. Mechanical Drawing of BDE-SG1314R10

4.2. PCB Footprints

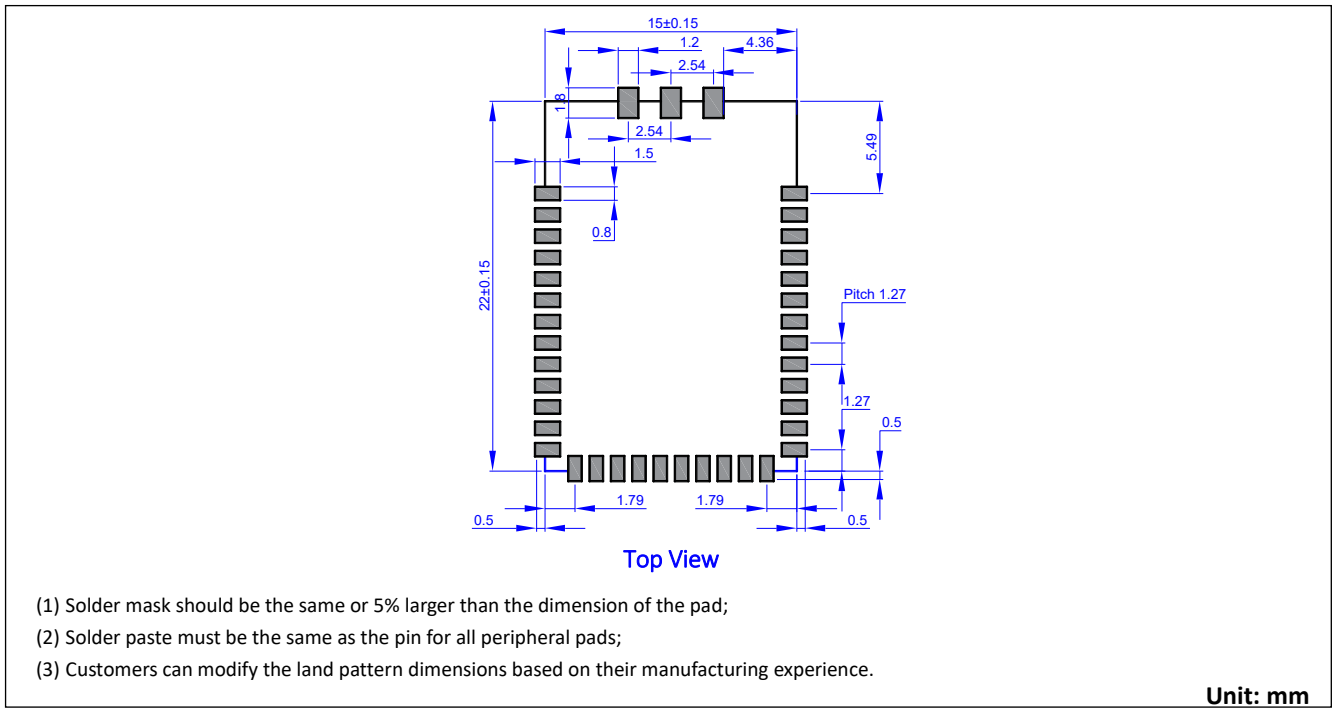
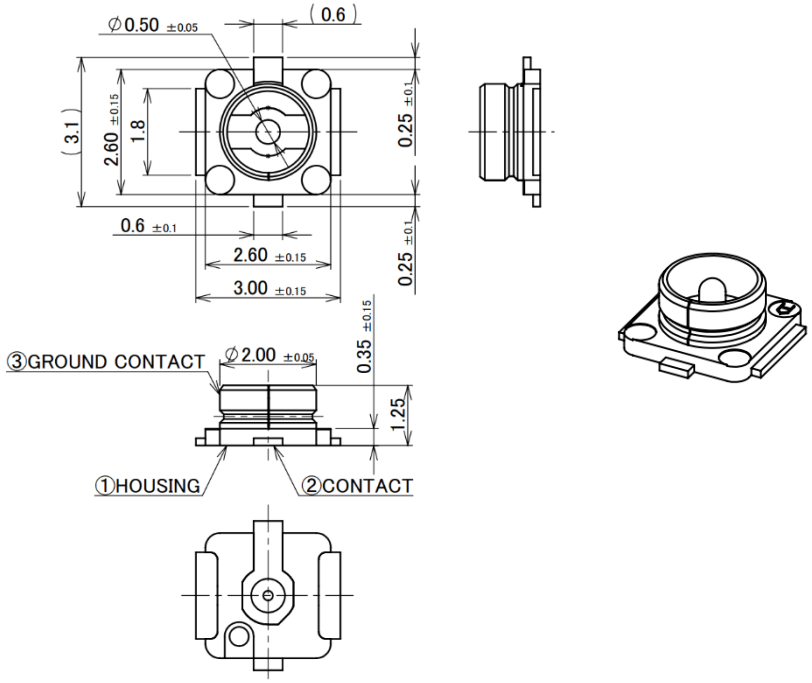


Figure 6. Recommended Module Footprint of BDE-SG1314R10

4.3. U.FL Connector Specification

The drawing and specification of the U.FL connector utilized in the module is as below for reference.

The dimension unit in below drawing is millimeter.



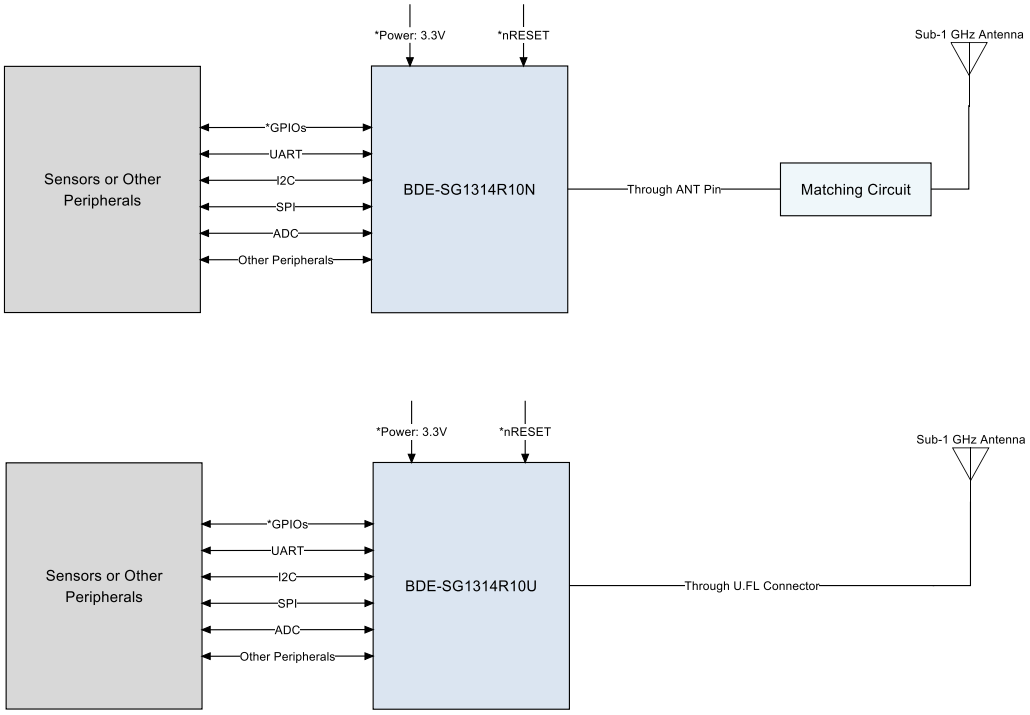
RATING VOLTAGE	60 V AC (R.M.S)	
RATING FREQUENCY	DC～9GHz	
OPERATING TEMPERATURE	233～363K (−40℃～+90℃)	
VSWR	RECEPTACLE: 1.3 MAX. AT 0.1～3 GHz, 1.4 MAX. AT 3～6 GHz, 1.8 MAX. AT 6～9 GHz	
MAIN CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 20 mohm MAX.	
GROUND CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 100 mohm MAX.	
INSULATION RESISTANCE	INITIAL: 500 Mohm MIN. / AFTER TEST: 100 Mohm MIN.	
DIELECTRIC WITHSTANDING VOLTAGE	200 V AC, 1 MINUTE	
DURABILITY	30 CYCLES	
UNMATING FORCE (INITIAL / AFTER TEST)	INITIAL: 5 N MIN. AFTER TEST: 3 N MIN.	INITIAL: 4 N MIN. AFTER TEST: 2 N MIN.

Figure 7. U.FL Connector Drawing and Specification

5. Integration Guideline

5.1. System Diagram

Below block diagram is applicable when the module is used as a SoC running the application and the protocol stack in the system CPU inside the module.



(1) The module has already been implemented with required decoupling capacitors, however, proper decoupling capacitors can also be added to increase module power stability depending on customer's application;
(2) The module has the internal reset circuit on board, e.g. a 100K ohm pull-up resistors and a 0.1uF decouple capacitor. Therefore, external reset circuit is not needed for the same purpose;
(3) If the SPI flash variant is chosen, please do not utilize these four GPIOs in your design, because they are already assigned to the on-board SPI flash. They are GPIO_8, GPIO_9, GPIO_10 and GPIO_20;
(4) It is recommended to reserve the matching circuit for antenna for tuning if the ANT pin version is chosen.

Figure 8. High-Level System Block Diagram

5.2. Module Placement

The placement of the module in the base board is critical in your design. Improper placement can lead to poor antenna performance. BDE recommend following below recommended placement in your design.

Any form of proximity to the metal or other material will change/degrade the antenna performance. Keep the antenna area as far as possible to the metal material in any direction.

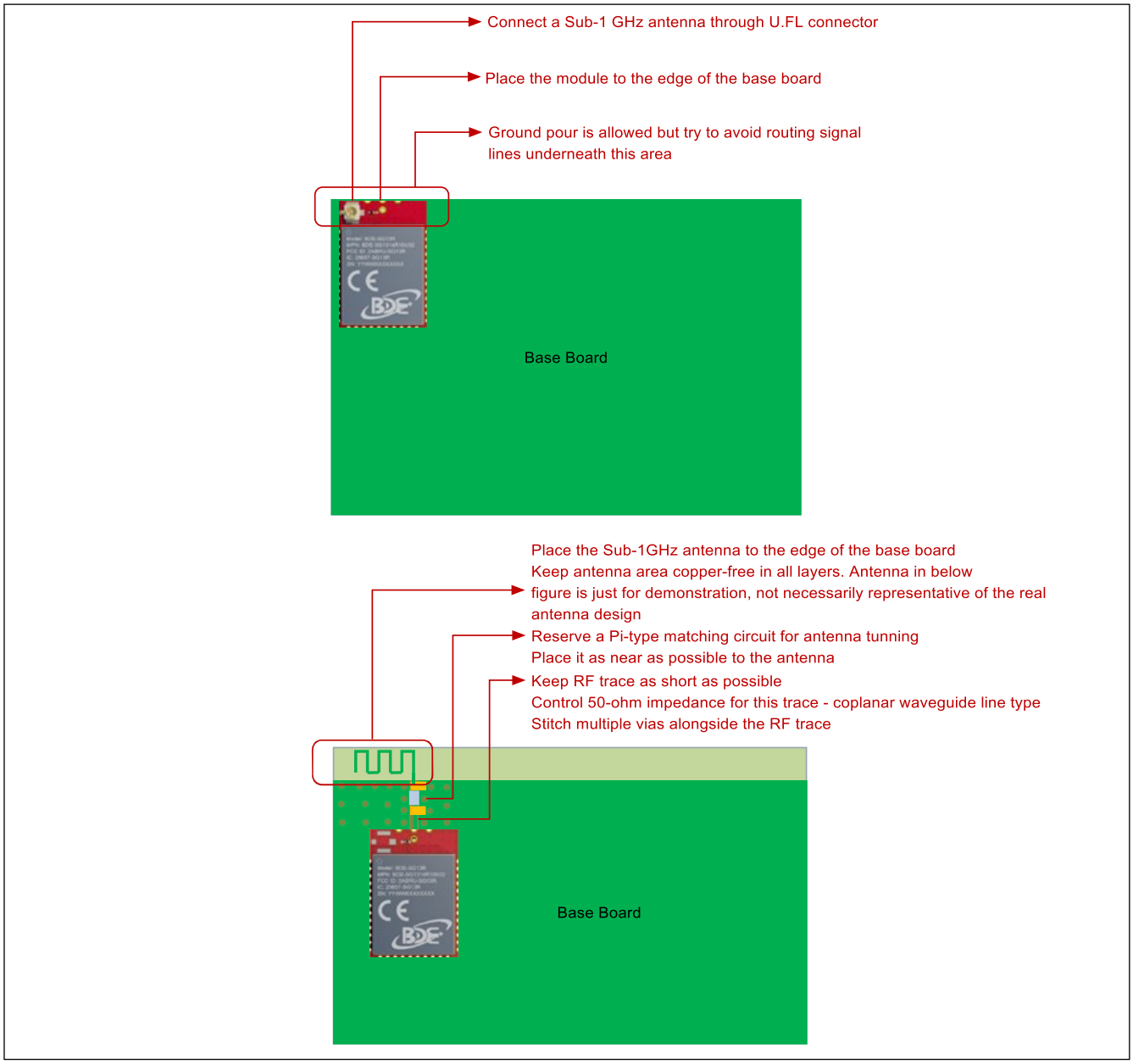


Figure 9. Module Placement Recommendations

5.3. Other Design Considerations

Table 24. Other Design Considerations

Thermal	
1	The proximity of ground vias must be close to each ground pad of the module.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to

	radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (50-ohm Coplanar or microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
14	BDE recommends using double-shielded coaxial RF cable to connect with the U.FL connector with antenna if the U.FL variants are selected.
15	Do not place or run the RF cable right above or below the module.
16	If there are some other radios besides this module in the system, try to place them apart as far as possible. And ensure there is at least 25 dB isolation between the antenna port of every radio.
Supply and Interface	
17	Make VDD traces as wide as possible to ensure reduced inductance and trace resistance.
18	If possible, shield VDD traces with ground above, below, and beside the traces.

5.4. Development Resources

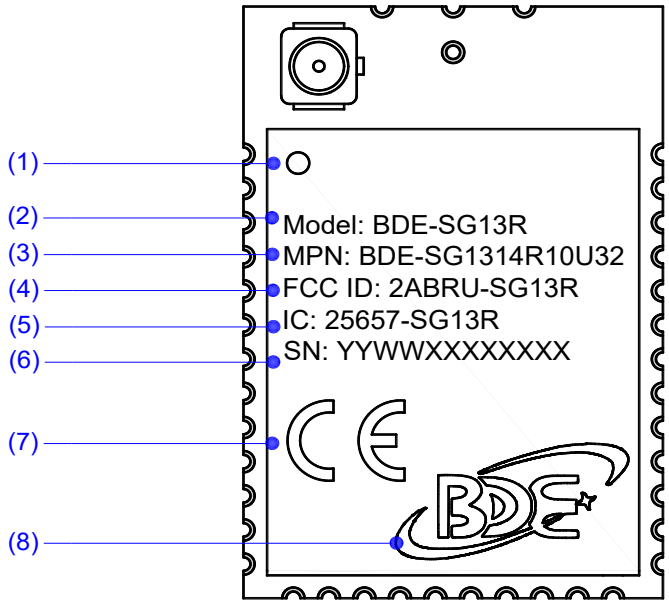
For more information on the EVK or other development resources, please visit the product page of the module on bdecomm.com.

6. Handling Instructions

The module is the surface mount module with LCC-39 footprint. It is designed to conform to the major manufacturing guidelines, including the commercial, industrial manufacturing process.

In this section, we will cover the basic shipping information, including the module markings, packaging, labeling, ect. And also, the instructions on how to handle the module in terms of storage, assembly and so on.

6.1. Module Marking

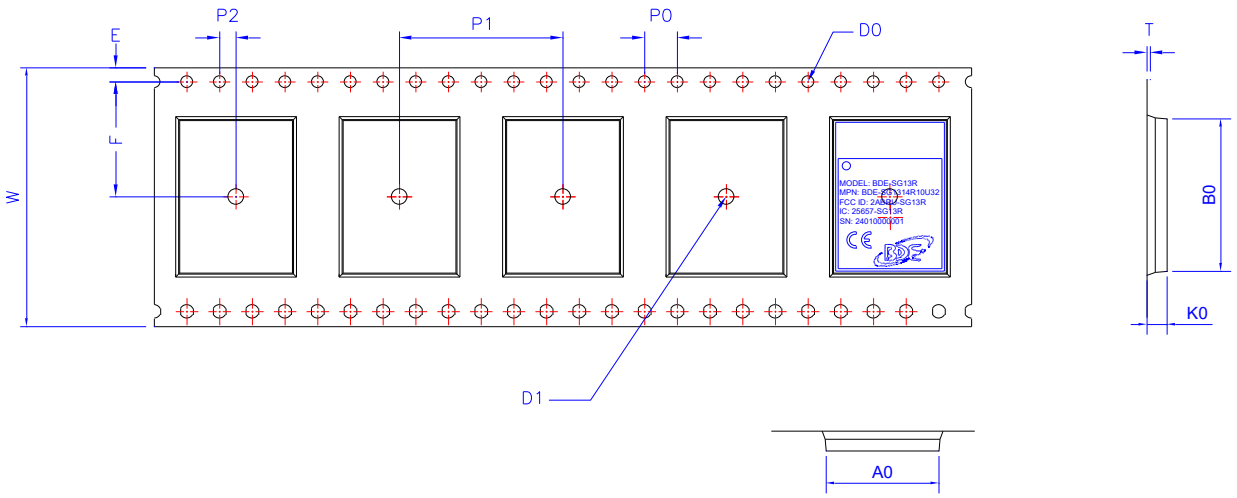


(1) Pin one index;
(2) Model series number;
(3) Orderable manufacturer part number. Refer to Table 1;
(4) FCC ID;
(5) IC ID;
(6) Serial number;
(7) CE marking;
(8) BDE logo

Figure 10. Module Marking

6.2. Packaging Information

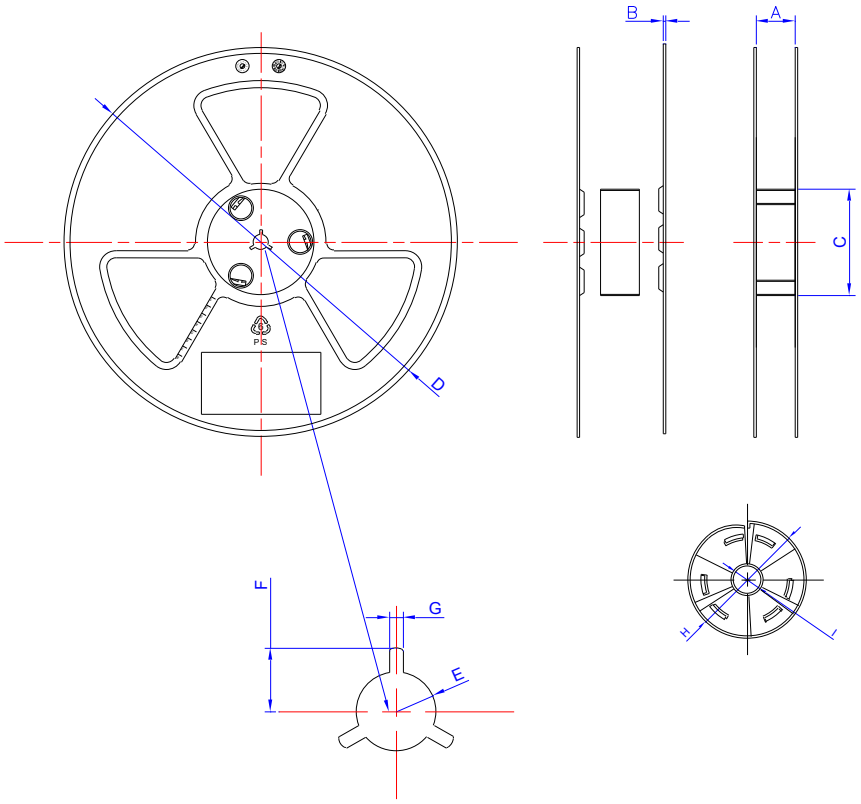
6.2.1. Tape and Reel Package Information



W	A_0	B_0	K_0	P_1	F	E	D_0	D_1	P_0	P_2	T
$44.00^{+0.30}_{-0.10}$	$15.35^{+0.10}_{-0.10}$	$22.45^{+0.10}_{-0.10}$	$2.50^{+0.10}_{-0.10}$	$20.00^{+0.10}_{-0.10}$	$20.20^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$2.00^{+0.10}_{-0.00}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$0.35^{+0.05}_{-0.05}$

(1) Cumulative tolerance for every 10 sprockets pitch is ±0.2mm;
(2) Carrier camber not to exceed 1mm in every 100mm;
(3) All dimensions are in millimeter and meets EIA-481-C requirements;
(4) Material: PS Black polystyrene;
(5) Thickness: 0.35±0.05mm;
(6) Packing length per 13"reel: 20.7 meters;
(7) Component load per 13"reel: 1000+30pcs (15 voids each to the head and tail);
(8) RoHS compliance;
(9) Anti-static coefficient of $10^{6-11}\Omega$.

Figure 11. Carrier Tape Drawing for BDE-SG1314R10 variants



A	B	C	D	E	F	G	H	I
44	2	100	330	6.75	10.85	2.5	100	24

(1) All dimensions are in millimeter;
(2) Material: PS blue polystyrene;

Figure 12. 13-INnch Reel Drawing

6.2.2. Carton Information and Labeling

6.2.2.1. Carton Information

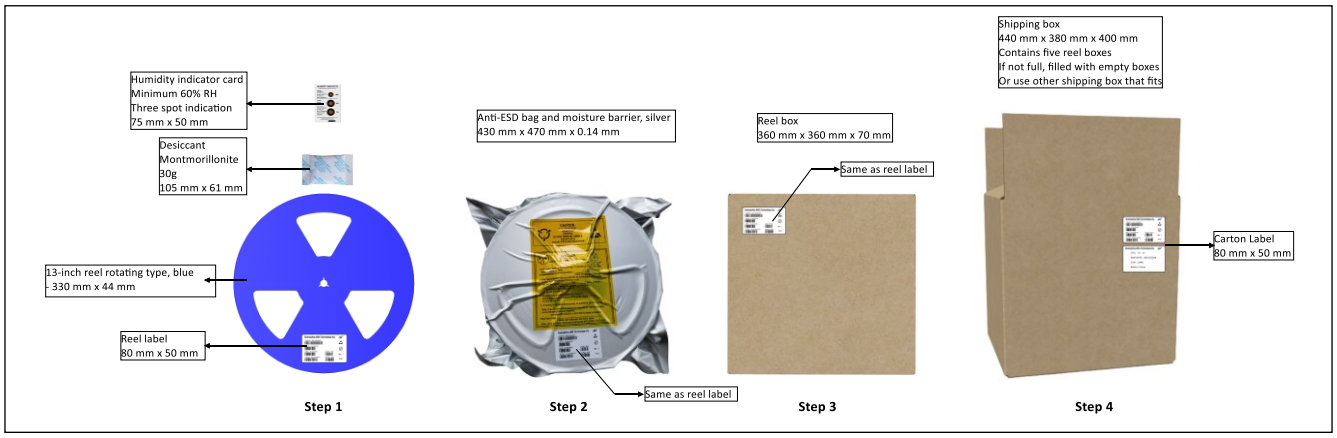


Figure 13. Carton Information

6.2.2.2. Reel Label

The reel label will be affixed onto the reel, Anti-ESD bag and reel box. It mainly shows the MPN (Manufacturer Part Number), CPN (Customer Part Number), PO (Purchase Order Number), LOT number, QTY (Quantity), DC (Date Code) and MSL (Moisture Sensitivity Level). Sometimes, it also shows other information, such as the regulatory information.

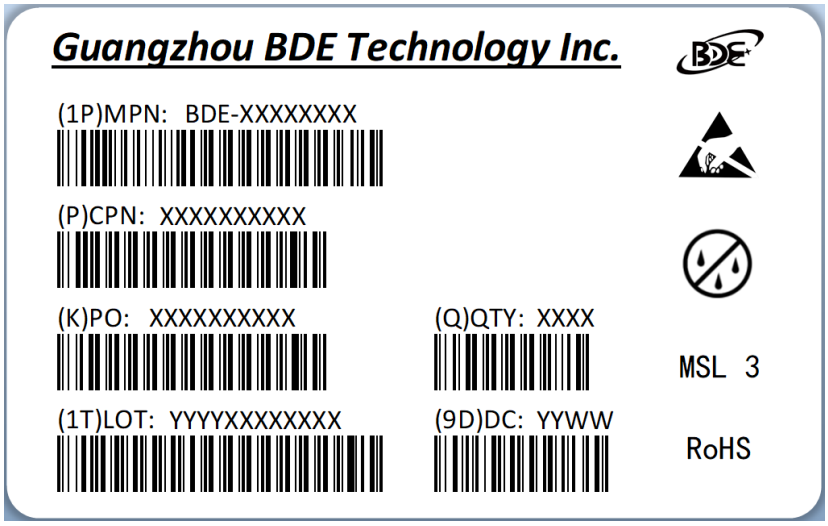


Figure 14. Reel Label Information

6.2.2.3. Carton Label

The carton label will be affixed onto the surface of the carton. If the carton contains different Part Numbers or POs, there will be different labels representing different Part Numbers, different Pos and Quantity.

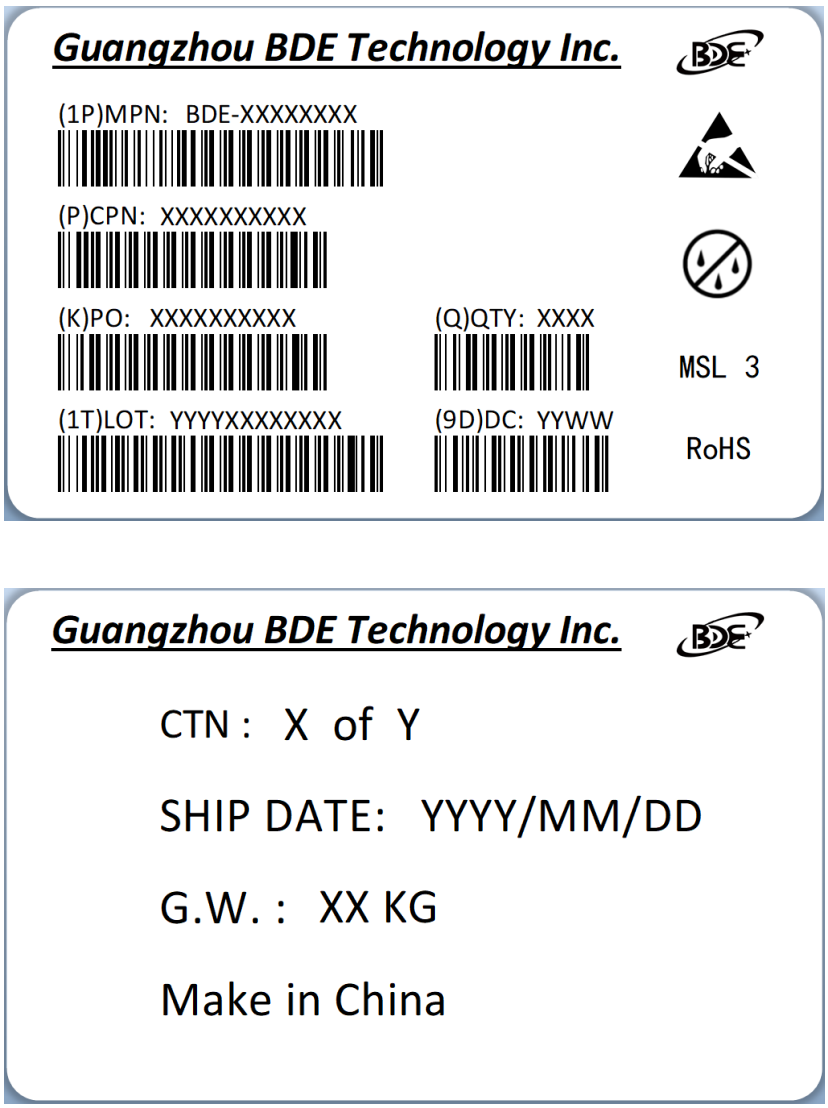


Figure 15. Carton Label Information

6.3. Assembly Instruction

6.3.1. Moisture Sensitive Level

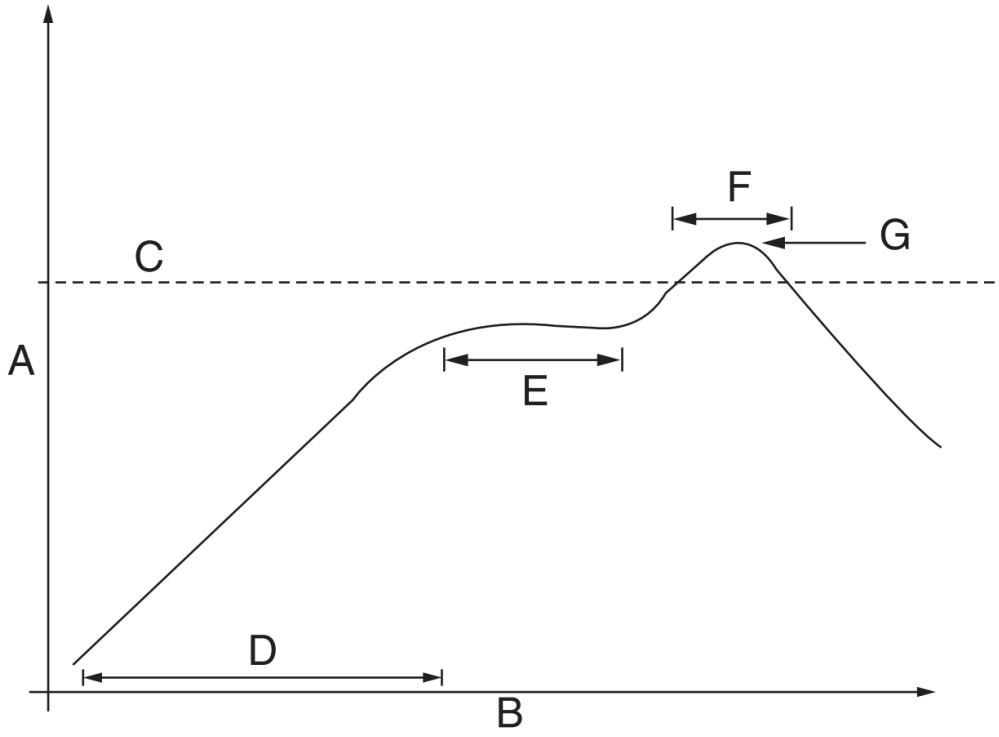
The MSL (Moisture Sensitive Level) of the module is MSL-3. Handling guidelines are listed as below:

(1) The floor life for MSL-3 device is 168 hours in ambient environment 30°C/60%RH. Before assembly, make sure to check if the modules are packaged with desiccate and humidity indicator card;

(2) After the bag is opened, make sure to mount the modules within 168 hours at factory conditions (< 30°C/60% RH) or stored at <10% RH. Repackage is needed with new desiccate and humidity indicator card if the modules are not mounted before exceeding floor life;

(3) If the card reads >10%, or the modules have been exposed for over 168 hours, the modules need to be baked before mounted. Recommended baking condition is 125℃ for 8 hours.

6.3.2. Reflow Profile



A – Temperature
B – Time
C – Alloy liquidus temperature
D – Preheat slope = temperature ramp rate
E – Preheat dwell = soak time
F – Time above liquidus
G – Peak temperature = maximum assembly temperature

Figure 16. Thermal Profile Schematic

Table 25. Reflow Profile Parameters [(1)] [(3)]

Item	Temperature Range	Ramp Rate / Time
D, preheat zone	30°C ~ 175°C	2°C ~ 4°C per second
E, soak zone	150°C ~ 200°C	60 ~ 120 seconds
C, Alloy liquidus temperature	217°C ~ 220°C	-
F, reflow zone	230°C ~ 245°C	60 ~ 90 seconds
G, target maximum reflow temperature	250°C	-
Absolute peak temperature [(2)]	260°C	-

(1) This is for Pb-free (SAC 305) paste. Different pastes require different profiles for optimum performance, so it is important to consult the paste manufacturer before developing the solder profile;
(2) Exceed the absolute peak temperature for certain period, e.g. 20s might damage the device or affect the reliability;
(3) It is recommended that the modules do not go through the reflow process more than one time.

6.3.3. Other Consideration

(1) Ultrasonic cleaning process is discouraged for the modules as the process might damage the module permanently, especially for the crystal oscillator in the module.
(2) Conformal coating is not allowed to this module. It will impact the reliability of the module once the coating flooded into the shield.

7. Certification

7.1. Regulatory Compliance

The module is certified for FCC, IC/ISED and ETSI/CE as listed in below table. More regions can be cover by request.

Table 26. Certification Information

Regulatory Body / Region	Standard	ID	MPN
FCC (USA)	FCC CFR 47 PART 15 C (15.247)	2ABRU-SG13R	BDE-SG1314R10U32 BDE-SG1314R10N32 BDE-SG1314R10U0 BDE-SG1314R10N0 BDE-SG1314R10U32-IN BDE-SG1314R10N32-IN BDE-SG1314R10U0-IN BDE-SG1314R10N0-IN
IC/ISED (Canada)	RSS-247 Issue 3 RSS-Gen Issue 5 ANSI C63.10: 2013	25657-SG13R	
ETSI/CE (Europe)	ETSI EN 301 489-1 V2.2.3 (2019-11) ETSI EN 301 489-3 V2.3.2 (2023-01) EN 55032:2015/A11:2020 EN 55035:2017/A11:2020 ETSI EN 300 220-1 V3.1.1 (2017-02) ETSI EN 300 220-2 V3.2.1 (2018-06) EN IEC 62311:2020 EN IEC 62368-1:2020+A11:2020	NA	

7.1.1. Certified Antennas

The module series has been tested and certified with a whip antenna; more antennas can be requested. Contact BDE sales team for more information.

The characteristic of the antenna is listed in below.

Table 27. Certified Antenna List

Antenna Type	Manufacturer	MPN	Peak Gain (dBi)	Note
Whip antenna	BDE	BDE-W89-20713-HRP	3.8	External

Customers are encouraged to use the certified antennas in the case of external antenna options to reduce certification testing effort and risk of failing. If customer want to choose another antenna that fits their product, there are some scenarios that need to be considered.

If the external antenna is of the same antenna type and of equal or less gain compared to the ones listed in above table, and with similar in-band and out-of-band characteristic, then the antenna can be used with the module in USA and Canada where modular approval is applicable, as long as the spot-check testing of the new antenna with host is performed to verified that

it will not change the performance. However, in countries such as EU countries applying the ETSI standards where the modular approval is not applicable, the radiated emissions are always tested with the end product with any antennas.

If the external antenna is of a different type or with non-similar in-band and out-of-band characteristic, but still has equal gain or less gain compared to the above listed antennas. The new antenna can be added to the existing modular grant/certificate by filing a permissive change, C2PC (Class II Permissive Change) in case of FCC and ISED. The radiated emission testing is needed, but re-certification is not required.

In the case of the external antenna with higher gain than the peak gain listed in above table are very likely to require a full new end product certification. However, we recommended that you consult with your certification house to understand the correct approaches for your product case by case.

7.1.2. FCC Compliance

7.1.2.1. FCC Statement

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and,
(2) This device must accept any interference received, including interference that may cause undesired operation.

7.1.2.2. FCC Caution

Any changes or modifications to this unit not expressly approved by BDE for compliance could void the user's authority to operate the equipment. The integrator will be responsible to satisfy SAR/RF Exposure requirements, when the module integrated into the host device.

7.1.2.3. Integration Instructions

List of applicable FCC rules
FCC Part 15.247

Specific operational use conditions
This transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

Limited module procedures
Not applicable

Trace antenna designs
Not applicable

RF exposure considerations
This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and minimum of 20cm separation between antenna and body. The host product manufacturer would provide the above information to end users in their end-product manuals.

Antennas
Refer to Table 27

Label and compliance information

The end product must carry a physical label or shall use e-labeling followed KDB784748D01 and KDB784748 stating “Contains Transmitter Module FCC ID: 2ABRU-SG13R”.

Information on test modes and additional testing requirements

Contact BDE for more information.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

(OEM) Integrator has to assure compliance of the entire end-product that includes the module. For 15 B (§15.107 and if applicable §15.109) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore, the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental/out-of-band). Finally, the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101. Integrator is reminded to assure that these installation instructions will not be made available to the end-user of the final host device.

7.1.3. IC/ISED Compliance

7.1.3.1. IC Statement

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada’s license-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and,

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L’émetteur/récepteur exempt de licencecontenudans le présentappareilestconforme aux CNR d’Innovation, Sciences et Développementéconomique Canada applicables aux appareils radio exempts de licence. L’exploitationestautorisée aux deux conditions suivantes :

(1) L' appareil ne doit pas produire de brouillage;

(2) L' appareildoit accepter tout brouillageradioélectriquesubi, mêmesi le brouillageest susceptible d' encompromettre le fonctionnement.

7.1.3.2. IC Caution

Any changes or modifications to this unit not expressly approved by BDE for compliance could void the user’s authority to operate the equipment. The integrator will be responsible to satisfy SAR/RF Exposure requirements, when the module integrated into the host device.

7.1.3.3. Integration Instructions

Label and compliance information

The final host device, into which this RF module is integrated has to be labeled with an auxiliary label stating the IC of the RF module, such as "Contains transmitter module IC: 25657-SG13R”.

Informations sur l'étiquette et la conformité

Le périphériquehôte final, danslequelce module RF estintégré "doitêtreétiqueté avec uneétiquetteauxiliaireindiquant le CI du module RF, tel que "Contient le module émetteur IC: 25657-SG13R”.

Radio Frequency Exposure Statement for IC

The device has been evaluated to meet general RF exposure requirements. The device can be used in mobile exposure conditions. The min separation distance is 20cm.

Déclaration d'exposition aux radiofréquences pour IC

L'appareil a été évalué pour répondre aux exigences générales en matière d'exposition aux RF. L'appareil peut être utilisé dans des conditions d'exposition mobiles. La distance de séparation minimale est de 20 cm.

This radio transmitter [IC: 25657-SG13R] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed in Table 27, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Cet émetteur radio [IC: 25657-SG13R] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste qui ont un gain supérieur au gain maximum indiqué pour tout type répertorié sont strictement interdits pour une utilisation avec cet appareil.

7.1.3.4. ETSI/CE Compliance

The module is certified with required EU radio and EMC directives. See Table 26 for detailed standards the module complies with.

8. Ordering Information

Table 28. Ordering Information

Part Number	Description	Size (mm)	Shipping Form	MOQ
BDE-SG1314R10U32	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with U.FL connector, with on-board 32Mbit SPI flash, -40℃ to +85℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10N32	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with ANT pin, with on-board 32Mbit SPI flash, -40℃ to +85℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10U0	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with U.FL connector, without on-board 32Mbit SPI flash, -40℃ to +85℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10N0	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with ANT pin, without on-board 32Mbit SPI flash, -40℃ to +85℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10U32-IN	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with U.FL connector, with on-board 32Mbit SPI flash, -40℃ to +105℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10N32-IN	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with ANT pin, with on-board 32Mbit SPI flash, -40℃ to +105℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10U0-IN	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with U.FL connector, without on-board 32Mbit SPI flash, -40℃ to +105℃	22 × 15 × 2.15	Tape & Reel	1K
BDE-SG1314R10N0-IN	BDE multi-protocol Sub-1GHz wireless module based on CC1314R106T0RGZ, with ANT pin in Sub-1GHz, without on-board 32Mbit SPI flash, -40℃ to +105℃	22 × 15 × 2.15	Tape & Reel	1K

9. Revision History

Table 29. Revision History

Revision	Date	Description
V0.1	30-Oc-2024	Preliminary, draft
V1.0	21-February-2025	Production version

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