BDE-BW3551

Datasheet V0.5

2.4GHz and 5GHz dual-band Wi-Fi 6 and Bluetooth 5.4 Low Energy wireless MCU module

- Based on TI's CC3551E
- 160MHz Arm®Cortex®-M33 processor with FPU, TrustZone®, and AI acceleration
- Flash upto 8MB
- Optional PSRAM upto 8MB
- Upto 27 GPIOs, supports 3.3V or 1.8V voltage level
- Integrated PCB trace antenna, U.FL connector or ANT pin
- Compact size

Contents

List of Figures

List of Tables

1. Overview

BDE-BW3551 module series is a 2.4GHz and 5GHz dual-band Wi-Fi 6 and Bluetooth 5.4 Low Energy wireless MCU module based on TI's SimpleLink™ Wi-Fi SoC (system-on-chip) CC3551E.

The module series offers the latest standards from Wi-Fi and Bluetooth Low Energy while maintaining compatibility with Wi-Fi 4 (802.11 a/b/g/n) and Wi-Fi 5 (802.11 ac).

The module series is an excellent choice to use in cost-sensitive embedded applications with RTOS software, bringing the efficiency of Wi-Fi 6 to embedded device applications for the Internet of Things (IoT), with a compact PCB footprint and highly optimized bill of materials.

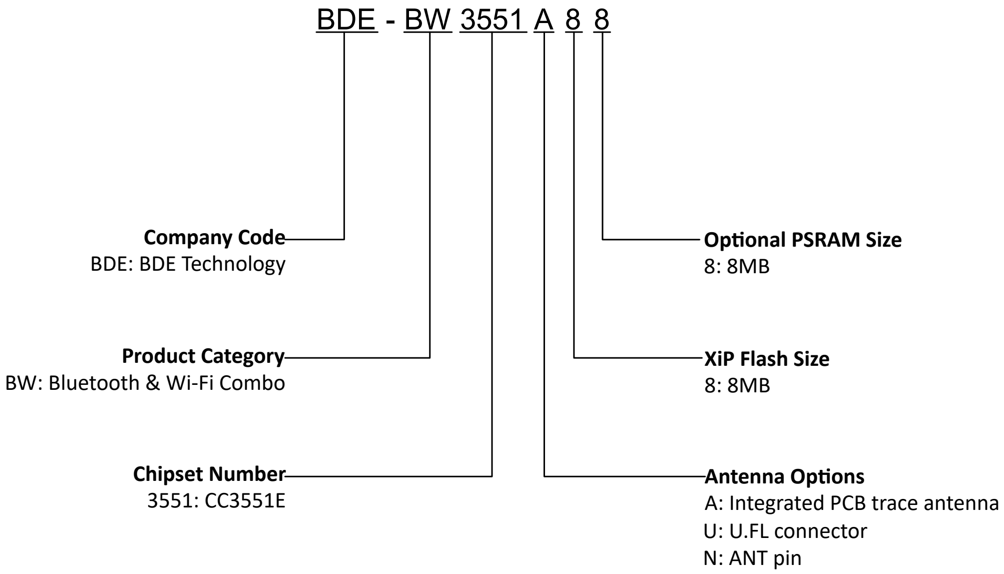
In order to meet different integration requirements, BDE offers different variants for this module series. They are listed in below table.

Table 1. Module Variants

MODEL SERIES	PART NUMBER	FLASH (MB)	OPTIONAL PSRAM (MB)	ANTENNA OPTIONS
BDE-BW355	BDE-BW3551A40	4	0	PCB trace antenna
	BDE-BW3551A80	8		
	BDE-BW3551A42	4	2	
	BDE-BW3551A82	8		
	BDE-BW3551A48	4	8	
	BDE-BW3551A88	8		
	BDE-BW3551U40	4	0	U.FL connector
	BDE-BW3551U80	8		
	BDE-BW3551U42	4	2	
	BDE-BW3551U82	8		
	BDE-BW3551U48	4	8	
	BDE-BW3551U88	8		
	BDE-BW3551N40	4	0	ANT pin
	BDE-BW3551N80	8		
	BDE-BW3551N42	4	2	
	BDE-BW3551N82	8		
	BDE-BW3551N48	4	8	
	BDE-BW3551N88	8		

The naming convention for be module variants is as follows:

Naming Convention of Module Variants



1.1. Features

Microcontroller

- Powerful 160MHz Arm®Cortex®-M33 processor with FPU, TrustZone®, and AI acceleration
- High-speed quad-SPI for XiP flash with on-the-fly decryption
- Flexible configuration of low-latency TCM (up to 32KB) and Cache (32KB or 64KB) for improved code execution performance
- 1.1MB embedded SRAM including 128KB TCM for Wi-Fi™, Bluetooth® Low Energy, networking, and application data

Peripherals

- Up to 27 I/Os with flexible multiplexing options
- 8x general-purpose timers and pulse-width modulation (PWM)
- 3x universal asynchronous receiver-transmitter (UART)
- 2x Serial Peripheral Interface (SPI)
- 2x inter-integrated circuit (I^2C)
- Inter-IC sound (I^2S)

- Pulse density modulation (PDM)
- Secure digital and multimedia card (SD/MMC)
- Secure digital input output (SDIO) 2.0
- Controller area network (CAN) 2.0
- 8-channel, 12-bit analog-to-digital converter (ADC)

System Services

- Direct memory access (DMA)
- One-time-programmable memory (OTP)
- Real-time clock (RTC) and watchdog timer (WDT)

Radio

- Wi-Fi 6 (802.11ax)
    - 2.4GHz and 5GHz, single-stream 20MHz channels with application throughput up to 20Mbps (UDP)
    - Compatible with IEEE 802.11 a/b/g/n/ax
        - Orthogonal frequency-division multiple access (OFDMA)
        - Target wake time (TWT)
        - Trigger frames
        - Basic service set (BSS) color
    - Integrated PA for a complete WLAN system with up to 18 dBm output power at 1 DSSS
    - Role support: STA, softAP , Wi-Fi direct, multi-role AP + STA
    - Support for personal and enterprise Wi-Fi security: WPA and WPA2 PSK, WPA2 Enterprise, WPA3 personal or enterprise
    - Wi-Fi TX Power:
        - 18 dBm at 1DSSS
        - 16 dBm at 54OFDM
    - Wi-Fi RX Sensitivity:
        - –96 dBm at 1DSSS
        - –74 dBm at 54OFDM
- Bluetooth® Low Energy
    - Bluetooth Low Energy 5.4 certified stack
    - Supports long-range and high-speed PHYs (up to 2Mbps)

Security Features

- ARM TrustZone
- Hardware security module supporting all of the following:

    - ECC, RSA, AES, SHA2/3, MD5, CRC 16/32, and TRNG
    - Secure key storage
- Initial secure programming
- Secure boot
- Software IP and cloning protection
- Debug security through JTAG and debug port lock
- OTP with the ability to program root-of-trust public key
- Secure over-the-air (OTA) updates
- Anti-rollback protection

Clock Source

- Fast clock: 52MHz XTAL
- Slow clock: Internal low-frequency oscillator, external 32.768kHz XTAL, or external slow clock source

Power Management

- Support for 3.3V and 1.8V on multiple I/O domains
- Supplies:
    - VDD_3V3: 3.3V
    - VDD_1V8: 1.8V
    - VDD_SF: 1.8V
    - VIO1: 1.8/3.3V
    - VIO2: 1.8/3.3V (Must be set to 1.8V for PSRAM variants)

Key Benefits

- Complete software development kit with open-source TCP/IP and TLS stacks
- Operating temperature: –40°C to +85°C
- Support for 3-wire PTA coexistence interface for use with external 2.4GHz radios (for example Thread or Zigbee®)
- Antenna selection capability

Memory

- Up to 8MB XiP flash

Antenna Options

- Integrated PCB trace antenna
- U.FL connector
- ANT pin

Package

- LGA-73, 14mm x 17.6mm x 2mm, PCB trace antenna variants
- LGA-73, 14mm x 16mm x 2mm, U.FL connector variants
- LGA-73, 14mm x 12.6mm x 2mm, ANT pin variants

Certifications - In-progress

- Bluetooth SIG
- FCC
- IC
- MIC
- CE-RED

1.2. Applications

- Building Automation
- Appliances
- Grid Infrastructure
- Medical
- Retail automation and payment
- Connected peripherals and printers
- Factory automation and control
- Asset tracking

2. Block Diagram

The module series is built around TI's wireless SoC CC3551E, as shown in below block diagram, depending on different configurations, is comprise of:

- CC3551E wireless SoC
- 52MHz XTAL
- Nor flash
- 2.4GHz band-pass filter
- 2.4GHz and 5GHz diplexer
- Decoupler capacitors
- PCB trace antenna/U.FL connector
- Other passives

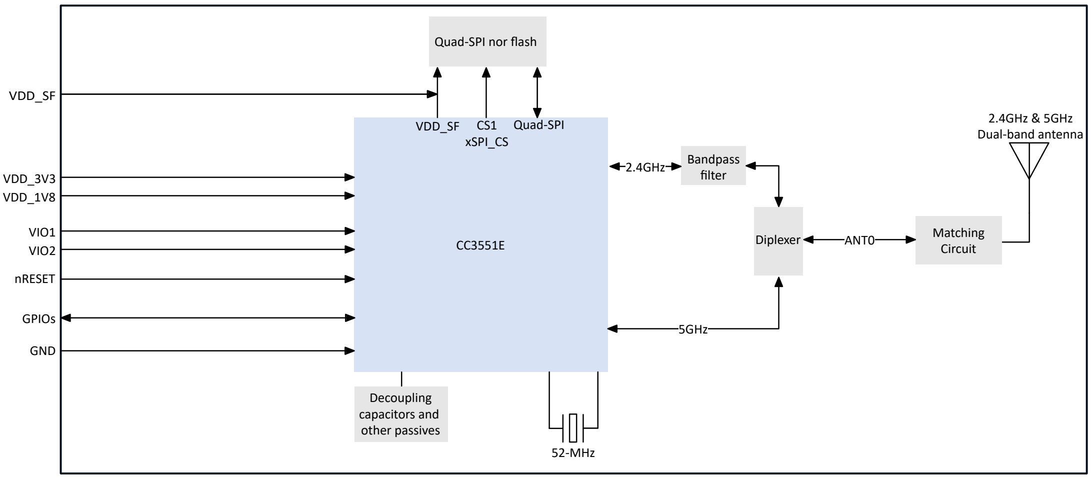


Figure 1. The Block Diagram of BDE-BW3551A Variants

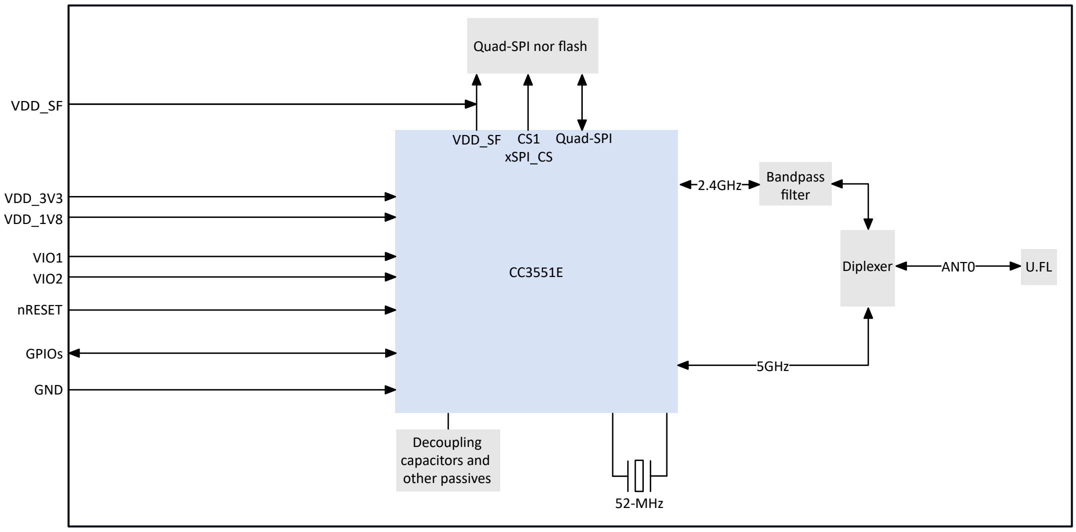


Figure 2. The Block Diagram of BDE-BW3551U Variants

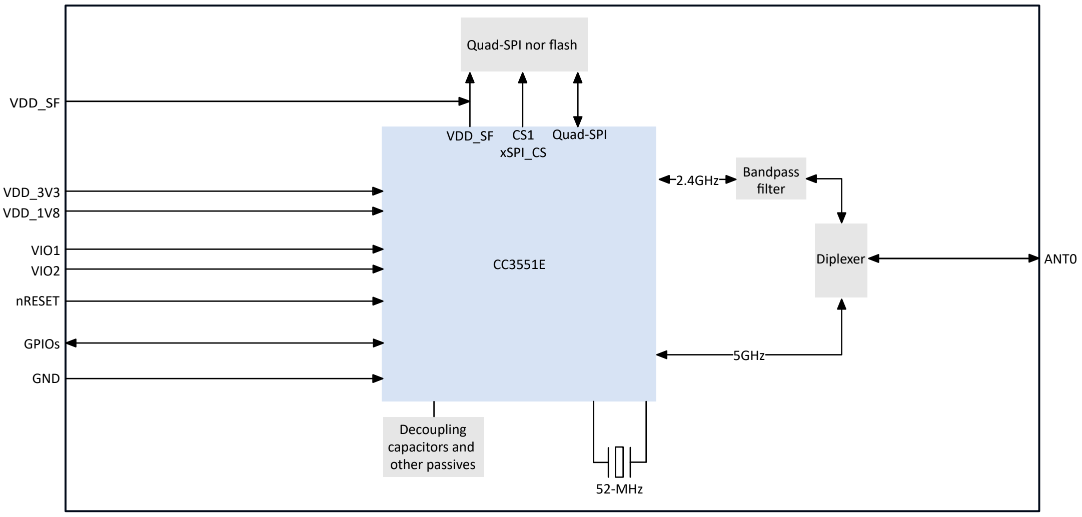


Figure 3. The Block Diagram of BDE-BW3551N Variants

3. Pin Functions

3.1. Pin Diagram

The pin diagrams of the module are shown as below figures.

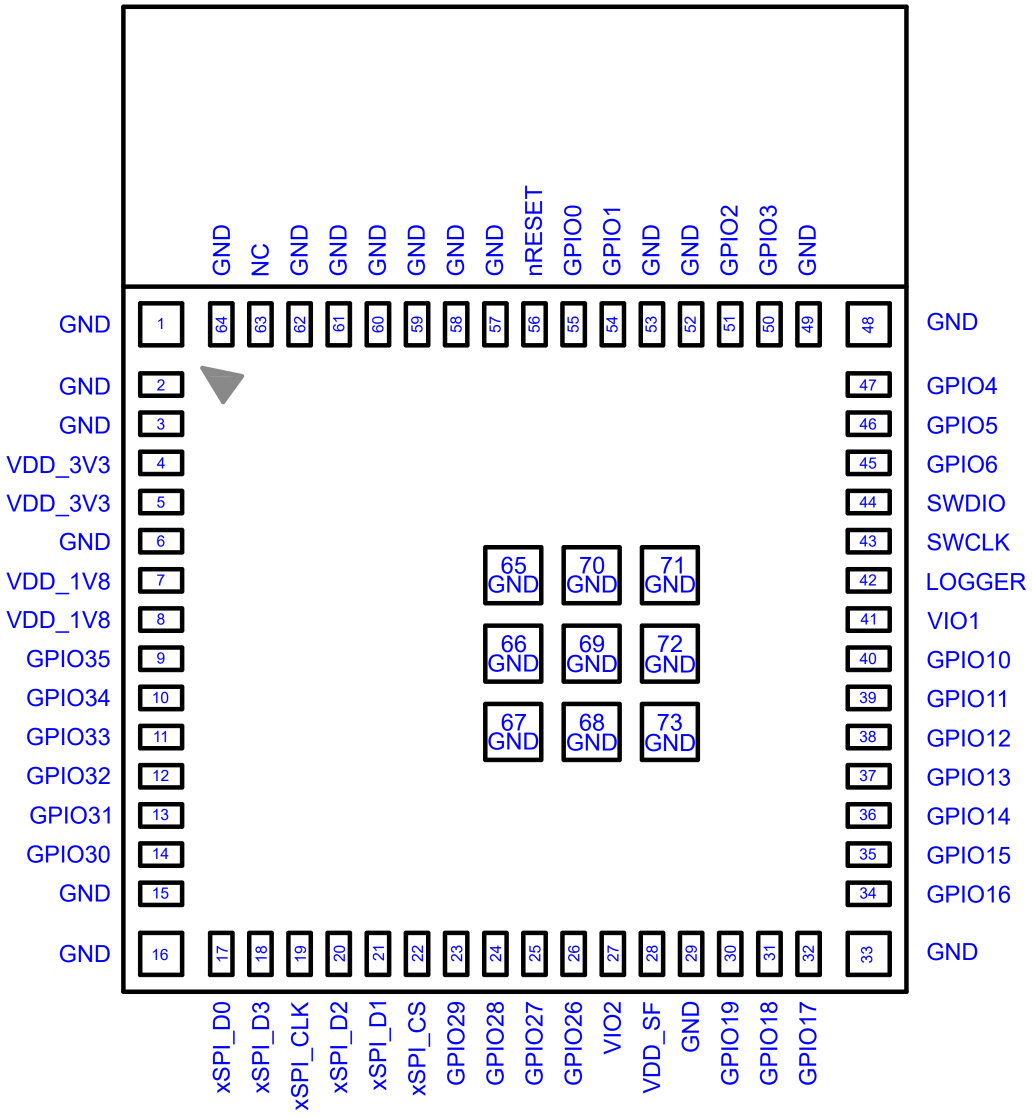


Figure 4. The Pin Diagram of BDE-BW3551A and BDE-BW3551U (Top Transparent View)

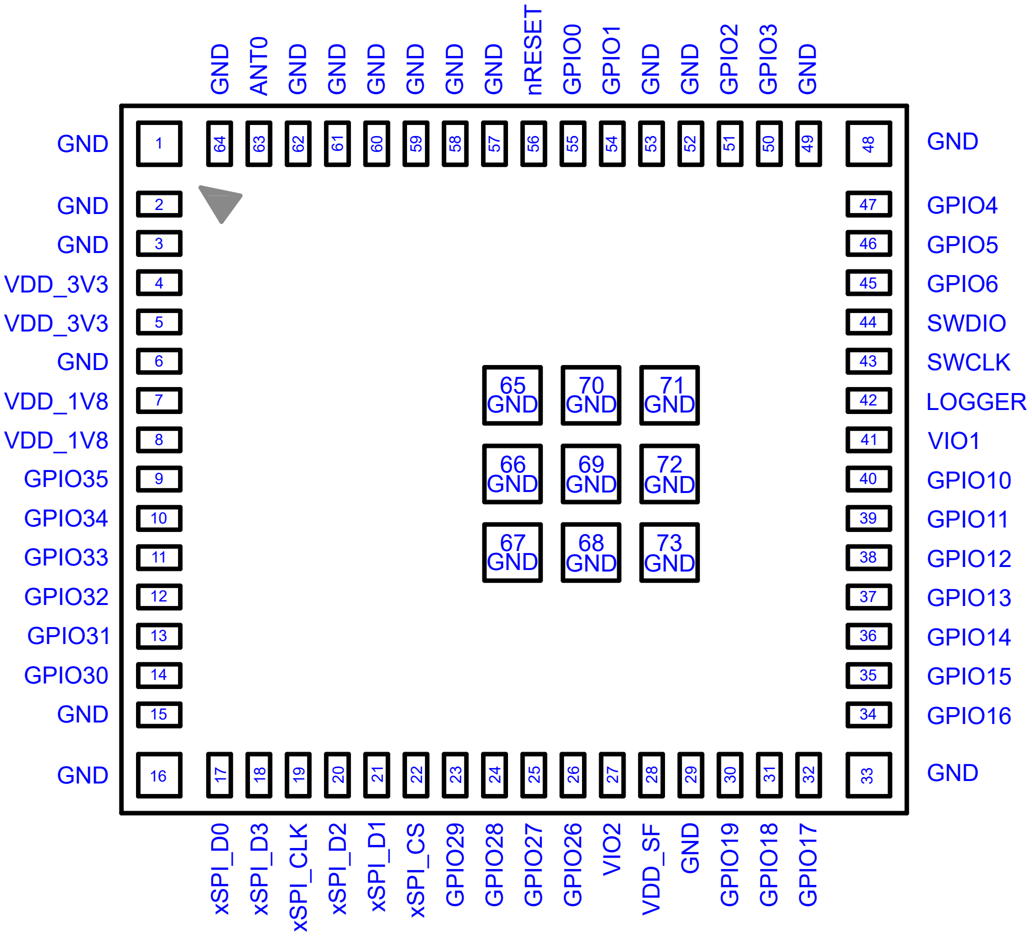


Figure 5. The Pin Diagram of BDE-BW3551N (Top Transparent View)

3.2. Pin Descriptions

Table 2. Pin Descriptions

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
1	-	GND	-	Ground	-	-	-	-
2	-	GND	-	Ground	-	-	-	-
3	-	GND	-	Ground	-	-	-	-
4	-	VDD_3V3	-	Power	-	-	-	-
5	-	VDD_3V3	-	Power	-	-	-	-

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
6	-	GND	-	Ground	-	-	-	-
7	-	VDD_1V8	-	Power	-	-	-	-
8	-	VDD_1V8	-	Power	-	-	-	-
9	8	GPIO35	SPI1_CLK	I/O	VIO2	3	PU	Hi-Z, Pull, Drive
			UART1_RX			5		
			I2C0_DATA			6		
			I2S_DATA1			7		
			PDM_BCLK			8		
			GPT0_1			9		
			DCAN_RX			10		
			I2C1_DATA			11		
			SPI0_CS4			16		
			SPI0_CS3			17		
			GPT0_2_N			18		
			GPT1_2_N			19		
			COEX_PRIORITY			20		
			ANT_SEL_0			23		
			GPT1_PRE_EVENT			24		
			COEX_REQ			29		
			SDIO_CMD			30		
			UART2_RX			31		
10	9	GPIO34	SPI1_PICO	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART1_CTS			5		
			I2C1_DATA			6		
			I2S_BCLK			7		
			PDM_DATA1			8		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			GPT1_3			9		
			DCAN_RX			10		
			SPI0_CS2			16		
			GPT1_1_N			18		
			GPT0_3_N			19		
			COEX_REQ			20		
			SDIO_CLK			30		
			UART2_RX			31		
11	11	GPIO33	SPI1_POCI	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART1_RX			5		
			I2C0_CLK			6		
			I2S_DATA0			7		
			PDM_DATA0			8		
			GPT1_2			9		
			DCAN_TX			10		
			SPI0_CS4			16		
			GPT1_0_N			18		
			GPT0_2_N			19		
			COEX_GRANT			20		
			GPT1_PRE_-EVENT			24		
			SDIO_D0			30		
			UART2_CTS			31		
12	12	GPIO32	SPI1_CS1	I/O	VIO2	3	PU	Hi-Z, Pull, Drive
			SPI1_CLK			4		
			UART1_TX			5		
			I2C0_DATA			6		
			I2S_DATA1			7		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			PDM_BCLK			8		
			GPT1_1			9		
			DCAN_RX			10		
			SPI0_CS3			16		
			GPT1_0_N			18		
			GPT0_1_N			19		
			COEX_REQ			20		
			SDIO_D1			30		
			UART2_RTS			31		
13	13	GPIO31	SPI1_CS1	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART1_RTS			5		
			I2C1_CLK			6		
			I2S_WCLK			7		
			PDM_BCLK			8		
			GPT1_0			9		
			DCAN_TX			10		
			SPI0_CS3			16		
			GPT1_1_N			18		
			GPT0_0_N			19		
			COEX_GRANT			20		
			ANT_SEL_0			23		
			GPT_INFRARED			24		
			SDIO_D2			30		
			UART2_TX			31		
14	14	GPIO30	I2C1_CLK	I/O	VIO2	5	PU	Hi-Z, Pull, Drive
			I2C0_CLK			6		
			I2S_DATA0			7		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			PDM_DATA0			8		
			GPT1_1			9		
			DCAN_TX			10		
			SPI0_CS2			16		
			GPT0_2_N			18		
			COEX_GRANT			19		
			COEX_REQ			20		
			ANT_SEL_0			23		
			CCA			24		
			GPT1_PRE_EVENT			28		
			GPT0_PRE_EVENT			29		
			SDIO_D3			30		
			UART2_TX			31		
15	-	GND	-	Ground	-	-	-	-
16	-	GND	-	Ground	-	-	-	-
17	20	xSPI_D0(3)	xSPI_D0	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
18	21	xSPI_D3(3)	xSPI_D3	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
19	22	xSPI_CLK(3)	xSPI_CLK	O	VDD_SF	-	PU	Hi-Z, Pull, Drive
20	24	xSPI_D2(3)	xSPI_D2	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
21	25	xSPI_D1(3)	xSPI_D1	I/O	VDD_SF	-	PU	Hi-Z, Pull, Drive
22	26	xSPI_CS(3)	xSPI_CS	O	VDD_SF	-	PU	1
23	16	GPIO29	SPI0_PICO	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART0_CTS			5		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			I2C1_DATA			6		
			I2S_BCLK			7		
			PDM_DATA1			8		
			GPT0_3			9		
			DCAN_RX			10		
			I2S_MCLK			12		
			SPI1_CS4			16		
			GPT0_1_N			18		
			GPT1_3_N			19		
			COEX_GRANT			20		
			SDIO_OOB_IRQ			30		
			UART2_RX			31		
24	17	GPIO28	SPI0_POCI	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART0_RX			5		
			I2C0_CLK			6		
			I2S_DATA1			7		
			PDM_BCLK			8		
			GPT0_2			9		
			SPI1_CS4			16		
			GPT0_0_N			18		
			GPT1_2_N			19		
			COEX_PRIORITY			20		
			GPT0_PRE_EVENT			24		
			UART2_CTS			31		
25	18	GPIO27	SPI0_CLK	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART0_TX			5		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			I2C0_DATA			6		
			I2S_DATA0			7		
			PDM_DATA0			8		
			GPT0_1			9		
			SPI1_CS3			16		
			GPT0_0_N			18		
			GPT1_1_N			19		
			COEX_REQ			20		
			UART2_RTS			31		
26	19	GPIO26	SPI0_CS1	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
			UART0_RTS			5		
			I2C1_CLK			6		
			I2S_WCLK			7		
			PDM_BCLK			8		
			GPT0_0			9		
			DCAN_TX			10		
			sSPI1_CS2			16		
			GPT0_1_N			18		
			GPT1_0_N			19		
			COEX_GRANT			20		
			COEX_REQ			21		
			ANT_SEL_0			23		
			GPT_INFRARED			24		
			SDIO_OOB_IRQ			30		
			UART2_TX			31		
27	-	VIO2(4)	-	Power	-	-	-	-

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
28	-	VDD_SF(4)	-	Power	-	-	-	-
29	-	GND	-	Ground	-	-	-	-
30	27	GPIO19	SPI0_PICO	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
			UART0_CTS			5		
			I2C1_CLK			6		
			I2S_BCLK			7		
			PDM_DATA0			8		
			GPT0_3			9		
			DCAN_RX			10		
			GPT0_PRE_EVENT			16		
			SDIO_OOB_IRQ			17		
			GPT0_1_N			18		
			SDIO_D3			19		
			COEX_PRIORITY			20		
			GPT1_3_N			21		
			GPT_INFRARED			22		
			UART2_RX			30		
31	28	GPIO18	SPI0_POCI	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
			UART0_RX			5		
			I2C0_DATA			6		
			I2S_DATA0			7		
			PDM_DATA1			8		
			GPT0_2			9		
			DCAN_TX			10		
			SPI1_CS4			16		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			SDIO_OOB_-IRQ			17		
			GPT0_0_N			18		
			COEX_REQ			20		
			GPT1_2_N			21		
32	29	GPIO17	SDMMC_WP	I/O	VIO1	1	PU	Hi-Z, Pull, Drive
			SPI0_CLK			4		
			UART0_TX			5		
			I2C0_CLK			6		
			I2S_DATA1			7		
			PDM_DATA0			8		
			GPT0_1			9		
			SPI1_CS3			16		
			SDIO_OOB_-IRQ			17		
			GPT0_0_N			18		
			COEX_GRANT			20		
			GPT1_1_N			21		
33	-	GND	-	Ground	-	-	-	-
34	30	GPIO16	SPI0_CS1	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
			UART0_RTS			5		
			I2C1_DATA			6		
			I2S_WCLK			7		
			PDM_BCLK			8		
			GPT0_0			9		
			SPI1_CS2			16		
			GPT0_1_N			18		
			SDIO_D2			19		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			GPT1_0_N			21		
			GPT_INFRARED			22		
			ANT_SEL_0			23		
			UART2_TX			30		
35	31	GPIO15	SDMMC_CMD	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
			SPI1_POCI			4		
			UART1_RX			5		
			UART0_CTS			6		
			GPT1_1			9		
			SPI0_CS2			16		
			GPT0_PRE_EVENT			17		
			GPT1_0_N			18		
			SDIO_D1			19		
			COEX_REQ			20		
36	32	GPIO14	SDMMC_CLK	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
			SPI1_CLK			4		
			UART1_TX			5		
			UART0_RX			6		
			GPT1_0			9		
			SPI0_CS2			16		
			GPT1_PRE_EVENT			17		
			GPT1_1_N			18		
			SDIO_D0			19		
			COEX_GRANT			20		
37	33	GPIO13	SDMMC_DATA_0	I/O	VIO1	3	PU	Hi-Z, Pull, Drive

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			SPI1_PICO			4		
			UART1_CTS			5		
			UART0_TX			6		
			I2S_BCLK			7		
			I2S_MCLK			8		
			GPT1_3			9		
			GPT1_2_N			18		
			SDIO_CMD			19		
			COEX_PRIORITY			20		
			ANT_SEL_0			23		
			UART2_RX			31		
38	34	GPIO12	SDMMC_DATA_1	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
			SPI1_CS1			4		
			UART1_RTS			5		
			UART0_RTS			6		
			I2S_WCLK			7		
			GPT1_2			9		
			GPT0_PRE_EVENT			16		
			GPT1_PRE_EVENT			17		
			GPT1_3_N			18		
			SDIO_CLK			19		
			UART2_TX			31		
39	35	GPIO11	ADC0	I/O	VIO1		PU	Hi-Z, Pull, Drive
			UART1_RX			1		
			SDMMC_DATA_2			3		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			SPI1_CS1			4		
			UART1_CTS			5		
			I2C1_CLK			6		
			I2S_DATA0			7		
			PDM_DATA0			8		
			GPT1_1			9		
			DCAN_TX			10		
			SPI0_CS2			16		
			GPT1_2_N			18		
			SDIO_D2			19		
			COEX_REQ			20		
			CCA			24		
			UART2_CTS			30		
			UART2_RX			31		
40	36	GPIO10	ADC1	I/O	VIO1		PU	Hi-Z, Pull, Drive
			UART1_TX			1		
			SDMMC_DATA_3			3		
			SPI1_CLK			4		
			UART1_RTS			5		
			I2C1_DATA			6		
			I2S_DATA1			7		
			PDM_DATA1			8		
			GPT1_0			9		
			DCAN_RX			10		
			SPI0_CS3			16		
			GPT1_3_N			18		
			SDIO_D3			19		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			COEX_PRIORITY			20		
			COEX_GRANT			21		
			CCA			24		
			UART2_RTS			30		
			UART2_TX			31		
41	-	VIO1 (4)	-	Power	-	-	-	-
42	38	LOGGER (5)	LOGGER	O	VIO1	-	PU	Hi-Z, Pull, Drive
43	39	SWCLK	SWCLK	I	VIO1	-	PD	Hi-Z, Pull, Drive
44	40	SWDIO	SWDIO	I/O	VIO1	-	PU	Hi-Z, Pull, Drive
45	41	GPIO6	ADC2	I/O	VIO1		PU	Hi-Z, Pull, Drive
			SDMMC_POW1			3		
			SPI1_PICO			4		
			UART1_RX			5		
			I2C0_DATA			6		
			I2S_WCLK			7		
			PDM_DATA0			8		
			GPT1_3			9		
			DCAN_RX			10		
			SDMMC_WP			11		
			SPI0_CS4			16		
			I2S_BCLK			17		
			GPT1_1_N			18		
			SDIO_D1			19		
			COEX_PRIORITY			20		
			GPT0_3_N			21		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			GPT1_PRE_-EVENT			22		
			ANT_SEL_0			23		
			CCA			24		
			COEX_GRANT			26		
			I2C1_CLK			28		
			SDMMC_POW2			29		
			UART2_CTS			30		
46	42	GPIO5	ADC3	I/O	VIO1		PU	Hi-Z, Pull, Drive
			SDMMC_POW2			3		
			SPI1_POCI			4		
			UART1_TX			5		
			I2C0_CLK			6		
			I2S_MCLK			7		
			PDM_BCLK			8		
			GPT1_2			9		
			DCAN_TX			10		
			SPI0_CS4			16		
			GPT1_0_N			18		
			SDIO_D0			19		
			COEX_REQ			20		
			GPT0_2_N			21		
			I2C1_DATA			28		
			UART2_RTS			30		
47	43	GPIO4	ADC4	I/O	VIO1		PU	Hi-Z, Pull, Drive
			UART1_RX			1		
			SDMMC_CD			3		
			SPI1_CS1			4		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			UART1_CTS			5		
			I2S_BCLK			6		
			I2S_DATA1			7		
			PDM_BCLK			8		
			GPT1_1			9		
			DCAN_TX			10		
			SPI0_CS2			16		
			GPT1_0_N			18		
			SDIO_CMD			19		
			COEX_PRIORITY			20		
			GPT0_1_N			21		
			I2C1_CLK			28		
			UART2_RX			30		
48	-	GND	-	Ground	-	-	-	-
49	-	GND	-	Ground	-	-	-	-
50	44	GPIO3	ADC5	I/O	VIO1		PU	Hi-Z, Pull, Drive
			UART1_TX			1		
			SDMMC_WP			3		
			SPI1_CLK			4		
			UART1_RTS			5		
			I2S_MCLK			6		
			I2S_DATA0			7		
			PDM_DATA1			8		
			GPT1_0			9		
			DCAN_RX			10		
			SPI0_CS3			16		
			GPT1_1_N			18		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			SDIO_CLK			19		
			COEX_REQ			20		
			GPT0_0_N			21		
			GPT_INFRARED			22		
			I2C1_DATA			28		
			UART2_TX			30		
51	46	GPIO2	ADC6	I/O	VIO1		PU	Hi-Z, Pull, Drive
			SDMMC_CD			3		
			I2C1_CLK			6		
			GPT1_3			9		
			DCAN_TX			10		
			SPI0_CS4			16		
			GPT1_PRE_EVENT			18		
			SDIO_OOB_IRQ			19		
			COEX_GRANT			20		
			COEX_REQ			21		
			CCA			24		
52	-	GND	-	Ground	-	-	-	-
53	-	GND	-	Ground	-	-	-	-
54	50	GPIO1	LFXTAL_N	I/O	VIO1	0	PD	Hi-Z, Pull, Drive
			ADC7					
			GPT1_PRE_EVENT			7		
			GPT0_PRE_EVENT			8		
			GPT1_0			9		
			GPT0_0			10		

Table 2. Pin Descriptions (continued)

MODULE PIN NO.	CHIP PIN NO.	PIN NAME	SIGNAL NAME	TYPE (1)	IO RING	PIN MUX ENCODING	PAD STATES	
							RESET	LPDS (2)
			GPT_IN-FRARED			11		
			SDIO_OOB_-IRQ			19		
			COEX_GRANT			20		
			COEX_REQ			21		
			ANT_SEL_0			23		
55	51	GPIO0	LFXTAL_P	I/O	VIO1		PD	Hi-Z, Pull, Drive
			SLOW_CLK_IN			1		
			GPT1_1			9		
			GPT0_1			10		
			COEX_REQ			21		
56	49	nRESET	nRESET	I	-	-	-	-
57	-	GND	-	Ground	-	-	-	-
58	-	GND	-	Ground	-	-	-	-
59	-	GND	-	Ground	-	-	-	-
60	-	GND	-	Ground	-	-	-	-
61	-	GND	-	Ground	-	-	-	-
62	-	GND	-	Ground	-	-	-	-
63	-	ANT0(6)	ANT	RF	-	-	-	-
64	-	GND	-	Ground	-	-	-	-
65 - 73	-	GND, thermal pads	-	Ground	-	-	-	-

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

(2) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

(3) SPI interface for on-module SFLASH, internal use only.

(4) VIO1 and VIO2 can be 1.8/3.3V optional for non-PSRAM variants. VIO2 must be set to 1.8V for PSRAM variants. VDD_SF must be set to 1.8V by default.

(5) Logger are sensed by the device during boot, boot state should be "1" with Logger being high.

(6) ANT0 is only for ANT variant.

3.3. Signal Descriptions

Table 3. Signal Descriptions

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
ADC	ADC0	GPIO11	35	VIO1	I	ADC channel 0 input
	ADC1	GPIO10	36			ADC channel 1 input
	ADC2	GPIO6	41			ADC channel 2 input
	ADC3	GPIO5	42			ADC channel 3 input
	ADC4	GPIO4	43			ADC channel 4 input
	ADC5	GPIO3	44			ADC channel 5 input
	ADC6	GPIO2	46			ADC channel 6 input
	ADC7	GPIO1	50			ADC channel 7 input
Antenna Select	ANT_SEL_0	GPIO1	50	VIO1	O	Antenna Selection Control
		GPIO37	52			
		GPIO6	41			
		GPIO13	33			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
		GPIO35	8			
Clear Channel Assesment	CCA	GPIO36	53	VIO1	O	Clear Channel Assesment Flag
		GPIO37	52			
		GPIO2	46			
		GPIO10	36			
		GPIO11	35			
		GPIO30	14	VIO2		
Clocks	SLOW_CLOCK_IN	GPIO0	51	VIO1	I	32.768kHz oscillator clock input or crystal LFXTAL_P pin

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
	LFXT_N	GPIO1	50	VIO1	N/A	32.768kHz crystal LFXTAL_N pin
Coexistence	COEX_REQ	GPIO0	51	VIO1	I	External Coexistence Interface - Request
		GPIO1	50			
		GPIO36	53			
		GPIO37	52			
		GPIO2	45			
		GPIO3	44			
		GPIO5	42			
		GPIO11	35			
		GPIO15	31			
		GPIO18	28			
		GPIO26	19	VIO2		
		GPIO27	18			
		GPIO30	14			
		GPIO32	12			
		GPIO34	9			
		GPIO35	8			
	COEX_GRANT	GPIO0	51	VIO1	O	External Coexistence Interface - Grant
		GPIO1	50			
		GPIO36	53			
		GPIO37	52			
		GPIO2	45			
		GPIO10	36			
		GPIO14	32			
		GPIO17	29			
		GPIO6	41			
		GPIO26	19	VIO2		
		GPIO29	16			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
		GPIO30	14			
		GPIO31	13			
		GPIO33	11			
	COEX_PRIORITY	GPIO4	43	VIO1	I	External Coexistence Interface - Priority
		GPIO41	6			
		GPIO10	36			
		GPIO13	33			
		GPIO19	27			
		GPIO28	17	VIO2		
		GPIO35	8			
DCAN	DCAN_TX	GPIO2	46	VIO1	O	Controller Area Network - TX
		GPIO4	43			
		GPIO5	42			
		GPIO11	35			
		GPIO18	28			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
		GPIO33	11			
	DCAN_RX	GPIO3	44	VIO1	I	Controller Area Network - RX
		GPIO6	41			
		GPIO10	36			
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO32	12			
		GPIO34	9			
		GPIO35	8			
GPIO	GPIO0		51	VIO1	I/O	General Purpose Inputs or Outputs

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
	GPIO1		50			
	GPIO36		53			
	GPIO37		52			
	GPIO2		45			
	GPIO3		44			
	GPIO4		43			
	GPIO5		42			
	GPIO6		41			
	GPIO10		36			
	GPIO11		35			
	GPIO12		34			
	GPIO13		33			
	GPIO14		32			
	GPIO15		31			
	GPIO16		30			
	GPIO17		29			
	GPIO18		28			
	GPIO19		27			
	GPIO26		19	VIO2		
	GPIO27		18			
	GPIO28		17			
	GPIO29		16			
	GPIO30		14			
	GPIO31		13			
	GPIO32		12			
	GPIO33		11			
	GPIO34		9			
	GPIO35		8			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[(1)]	DESCRIPTION
I^2C	I2C0_CLK	GPIO5	42	VIO1	I/O	I^2C0 Clock SCL
		GPIO17	29			
		GPIO28	17	VIO2		
		GPIO30	14			
		GPIO33	11			
	I2C0_DATA	GPIO6	41	VIO1	I/O	I^2C0 Data SDA
		GPIO18	28			
		GPIO27	18	VIO2		
		GPIO32	12			
		GPIO35	8			
	I2C1_CLK	GPIO2	45	VIO1	I/O	I^2C1 Clock SCL
		GPIO4	43			
		GPIO6	41			
		GPIO11	35			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
	I2C1_DATA	GPIO3	44	VIO1	I/O	I^2C1 Data SDA
		GPIO5	42			
		GPIO10	36			
		GPIO16	30			
		GPIO29	16	VIO2		
		GPIO34	9			
		GPIO35	8			
I^2S	I2S_DATA0	GPIO3	44	VIO1	I/O	I^2S Audio Port Data 0
		GPIO11	35			
		GPIO18	28			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
		GPIO27	18	VIO2		
		GPIO33	11			
	I2S_DATA1	GPIO4	43	VIO1	I/O	I^{2}S Audio Port Data 1
		GPIO10	36			
		GPIO17	29			
		GPIO28	17	VIO2		
		GPIO32	12			
		GPIO35	8			
	I2S_WCLK	GPIO6	41	VIO1	I	I^{2}S Audio Port Word Transfer Clock
		GPIO12	34			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO31	13			
	I2S_BCLK	GPIO4	43	VIO1	I	I^{2}S Audio Port Bit Clock
		GPIO13	33			
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO34	9			
	I2S_MCLK	GPIO3	44	VIO1	O	I^{2}S Audio Port Controller Clock
		GPIO5	42			
		GPIO6	41			
		GPIO13	33			
		GPIO29	16	VIO2		
Logger		-	38	VIO1	O	Tracer (UART TX Debug Logger)
xSPI	xSPI_CLK	-	21	VD-DSF	O	Clock to xSPI Flash/RAM
	xSPI_DATA_0	-	20		I/O	Data 0 to xSPI Flash/RAM
	xSPI_DATA_1	-	25		I/O	Data 1 to xSPI Flash/RAM
	xSPI_DATA_2	-	24		I/O	Data 2 to xSPI Flash/RAM

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
	xSPI_DATA_3	-	22		I/O	Data 3 to xSPI Flash/RAM
	xSPI_CS_FLASH	-	26	VDDSF	O	Chip select to xSPI Flash
PDM	PDM_Data0	GPIO6	41	VIO1	I	Pulse Density Modulation Data 0
		GPIO11	35			
		GPIO17	29			
		GPIO19	27			
		GPIO27	18	VIO2		
		GPIO30	14			
		GPIO33	11			
	PDM_Data1	GPIO3	44	VIO1	I	Pulse Density Modulation Data 1
		GPIO10	36			
		GPIO18	28			
		GPIO29	16	VIO2		
		GPIO34	9			
	PDM_BCLK	GPIO4	43	VIO1	O	Pulse Density Modulation Clock
		GPIO5	42			
		GPIO16	30			
		GPIO28	17	VIO2		
		GPIO31	13			
		GPIO32	12			
		GPIO35	8			
Power	VDD_3V3	-	-	N/A	N/A	3.3V supply
	VDD_1V8	-	-	N/A	N/A	1.8V supply
	VIO1	-	-	N/A	N/A	1.8/3.3V IO supply for IO Ring 1
	VIO2	-	-	N/A	N/A	1.8/3.3V IO supply for IO Ring 2
nReset		-	49	N/A	N/A	Reset line for enabling or disabling device (active low)
RF	ANT0	-	-	N/A	N/A	Antenna port 0

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
SDIO	SDIO_CLK	GPIO3	44	VIO1	I	SDIO Clock
		GPIO12	34			
		GPIO34	9	VIO2		
	SDIO_CMD	GPIO4	43	VIO1	I/O	SDIO Command
		GPIO13	33			
		GPIO35	8	VIO2		
	SDIO_D0	GPIO5	42	VIO1	I/O	SDIO Data 0
		GPIO14	32			
		GPIO33	11	VIO2		
	SDIO_D1	GPIO6	41	VIO1	I/O	SDIO Data 1
		GPIO15	31			
		GPIO32	12	VIO2		
	SDIO_D2	GPIO11	35	VIO1	I/O	SDIO Data 2
		GPIO16	30			
		GPIO31	13	VIO2		
	SDIO_D3	GPIO10	36	VIO1	I/O	SDIO Data 3
		GPIO19	27			
		GPIO30	14	VIO2		
	SDIO_OOB_-IRQ	GPIO1	51	VIO1	O	SDIO out of band interrupt
		GPIO37	52			
		GPIO2	45			
		GPIO17	29			
		GPIO18	28			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO29	16			
SDMMC	SDMMC_CLK	GPIO14	32	VIO1	O	SDMMC Clock
	SDMMC_CMD	GPIO15	31	VIO1	I/O	SDMMC Command

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
	SDMMC_DATA_0	GPIO13	33	VIO1	I/O	SDMMC Data 0
	SDMMC_DATA_1	GPIO12	34	VIO1	I/O	SDMMC Data 1
	SDMMC_DATA_2	GPIO11	35	VIO1	I/O	SDMMC Data 2
	SDMMC_DATA_3	GPIO10	36	VIO1	I/O	SDMMC Data 3
	SDMMC_CD	GPIO2	45	VIO1	I	SDMMC Card Detect
		GPIO4	43			
	SDMMC_WP	GPIO36	53	VIO1	I	SDMMC Write Protect
		GPIO37	52			
		GPIO3	43			
		GPIO6	41			
		GPIO11	41			
		GPIO17	29			
	SDMMC_POW1	GPIO37	52	VIO1	O	SDMMC power supply control 1
		GPIO6	41			
	SDMMC_POW2	GPIO36	53	VIO1	O	SDMMC power supply control 2
		GPIO5	42			
SPI	SPI0_CLK	GPIO17	29	VIO1	I/O	General SPI0 Clock
		GPIO27	18	VIO2		
	SPI0_POCI	GPIO18	28	VIO1	I/O	General SPI0 POCI
		GPIO28	17	VIO2		
	SPI0_PICO	GPIO19	27	VIO1	I/O	General SPI0 PICO
		GPIO29	16	VIO2		
	SPI0_CS1	GPIO16	30	VIO1	I/O	General SPI0 Chip select 1
		GPIO26	19	VIO2		
	SPI0_CS2	GPIO4	43	VIO1	I/O	General SPI0 Chip select 2
		GPIO11	35			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
		GPIO14	32			
		GPIO30	14	VIO2		
		GPIO34	9			
	SPI0_CS3	GPIO3	34	VIO1	I/O	General SPI0 Chip select 3
		GPIO10	36			
		GPIO31	13	VIO2		
		GPIO32	12			
	SPI0_CS4	GPIO2	45	VIO1	I/O	General SPI0 Chip select 4
		GPIO5	42			
		GPIO6	41			
		GPIO33	11	VIO2		
		GPIO35	8			
	SPI1_CLK	GPIO3	44	VIO1	I/O	General SPI1 Clock
		GPIO10	36			
		GPIO14	32			
		GPIO32	12	VIO2		
		GPIO35	8			
	SPI1_POCI	GPIO5	42	VIO1	I/O	General SPI1 POCI
		GPIO15	31			
		GPIO33	11	VIO2		
	SPI1_PICO	GPIO6	41	VIO1	I/O	General SPI1 PICO
		GPIO13	33			
		GPIO34	19	VIO2		
	SPI1_CS1	GPIO4	43	VIO1	I/O	General SPI1 Chip select 1
		GPIO11	35			
		GPIO12	34			
		GPIO31	13	VIO2		
		GPIO32	12			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
	SPI1_CS2	GPIO15	32	VIO1	I/O	General SPI1 Chip select 2
		GPIO16	30			
		GPIO26	19	VIO2		
	SPI1_CS3	GPIO17	29	VIO1	I/O	General SPI1 Chip select 3
		GPIO27	18	VIO2		
SPI	SPI1_CS4	GPIO18	28	VIO1	I/O	General SPI1 Chip select 4
		GPIO28	17	VIO2		
		GPIO29	16			
SWD	SWDIO	-	40	VIO1	I/O	Serial Wire Debug I/O
	SWCLK	-	39		I	Serial Wire Debug Clock
Timers_0	GPT0_0	GPIO1	50	VIO1	I/O	General Purpose Timer 0 Channel 0
		GPIO16	30			
		GPIO26	19	VIO2		
	GPT0_1	GPIO0	51	VIO1	I/O	General Purpose Timer 0 Channel 1
		GPIO17	29			
		GPIO27	18	VIO2		
		GPIO35	8			
	GPT0_2	GPIO18	28	VIO1	I/O	General Purpose Timer 0 Channel 2
		GPIO28	17	VIO2		
	GPT0_3	GPIO19	27	VIO1	I/O	General Purpose Timer 0 Channel 3
		GPIO29	16	VIO2		
	GPT0_0_N	GPIO3	44	VIO1	I/O	General Purpose Timer 0 Channel 0 Negative
		GPIO17	29			
		GPIO18	28			
		GPIO27	18	VIO2		
		GPIO28	17			
		GPIO31	13			
	GPT0_1_N	GPIO4	43	VIO1	I/O	General Purpose Timer 0 Channel 1 Negative

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
		GPIO16	30			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO29	16			
		GPIO32	12			
	GPT0_2_N	GPIO5	42	VIO1	I/O	General Purpose Timer 0 Channel 2 Negative
		GPIO30	14	VIO2		
		GPIO33	11			
		GPIO35	8			
	GPT0_3_N	GPIO6	41	VIO1	I/O	General Purpose Timer 0 Channel 3 Negative
		GPIO34	9	VIO2		
	GPT0_PRE_-EVENT	GPIO1	50	VIO1	O	General Purpose Timer 0 PreEvent Signal
		GPIO12	34			
		GPIO15	31			
		GPIO19	27			
		GPIO28	17	VIO2		
		GPIO30	14			
Timers_1	GPT1_0	GPIO1	50	VIO1	I/O	General Purpose Timer 1 Channel 0
		GPIO3	44			
		GPIO10	35			
		GPIO14	32			
		GPIO31	13	VIO2		
	GPT1_1	GPIO0	51	VIO1	I/O	General Purpose Timer 1 Channel 1
		GPIO4	43			
		GPIO11	35			
		GPIO15	31			
		GPIO30	14	VIO2		
		GPIO32	12			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
	GPT1_2	GPIO5	42	VIO1	I/O	General Purpose Timer 1 Channel 2
		GPIO12	34			
		GPIO33	11	VIO2		
	GPT1_3	GPIO2	45	VIO1	I/O	General Purpose Timer 1 Channel 3
		GPIO6	41			
		GPIO13	33			
		GPIO34	9	VIO2		
	GPT1_0_N	GPIO4	43	VIO1	I/O	General Purpose Timer 1 Channel 0 Negative
		GPIO5	42			
		GPIO15	31			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO32	12			
		GPIO33	11			
	GPT1_1_N	GPIO3	44	VIO1	I/O	General Purpose Timer 1 Channel 1 Negative
		GPIO6	41			
		GPIO14	32			
		GPIO17	29			
		GPIO27	18	VIO2		
		GPIO31	13			
		GPIO34	9			
	GPT1_2_N	GPIO11	35	VIO1	I/O	General Purpose Timer 1 Channel 2 Negative
		GPIO13	33			
		GPIO18	28			
		GPIO28	17	VIO2		
		GPIO35	8			
	GPT1_3_N	GPIO10	36	VIO1	I/O	General Purpose Timer 1 Channel 3 Negative
		GPIO12	34			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
		GPIO19	27			
		GPIO29	16	VIO2		
Timers_1	GPT1_PRE_-EVENT	GPIO1	50	VIO1	O	General Purpose Timer 1 PreEvent Signal
		GPIO2	45			
		GPIO6	41			
		GPIO12	34			
		GPIO14	32			
		GPIO33	11	VIO2		
		GPIO35	8			
Timers_Infrared	GPT_IN-FRARED	GPIO1	50	VIO1	O	General Purpose Timer Infrared Signal
		GPIO3	44			
		GPIO16	30			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO31	13			
UART	UART0_TX	GPIO13	33	VIO1	O	UART0 TX
		GPIO17	29			
		GPIO27	18	VIO2		
	UART0_RX	GPIO14	32	VIO1	I	UART0 RX
		GPIO18	28			
		GPIO28	17	VIO2		
	UART0_RTS	GPIO12	34	VIO1	O	UART0 request to send
		GPIO16	30			
		GPIO26	19	VIO2		
	UART0_CTS	GPIO15	31	VIO1	I	UART0 clear to send
		GPIO19	27			
		GPIO29	16	VIO2		
	UART1_TX	GPIO3	44	VIO1	O	UART1 TX

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR(1)	DESCRIPTION
		GPIO5	42			
		GPIO10	36			
		GPIO14	32			
		GPIO32	12	VIO2		
	UART1_RX	GPIO4	43	VIO1	I	UART1 RX
		GPIO6	41			
		GPIO11	35			
		GPIO15	31			
		GPIO33	11	VIO2		
		GPIO35	8			
	UART1_RTS	GPIO3	44	VIO1	O	UART1 request to send
		GPIO10	36			
		GPIO12	34			
		GPIO31	13	VIO2		
	UART1_CTS	GPIO4	43	VIO1	I	UART1 clear to send
		GPIO11	35			
		GPIO13	33			
		GPIO34	9	VIO2		
UART	UART2_TX	GPIO3	44	VIO1	O	UART2 TX
		GPIO10	36			
		GPIO12	34			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
	UART2_RX	GPIO4	43	VIO1	I	UART2 RX
		GPIO11	35			
		GPIO13	33			

Table 3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	CHIP PIN NO.	IO RING	DIR[1]	DESCRIPTION
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO34	9			
		GPIO35	8			
	UART2_RTS	GPIO5	42	VIO1	O	UART2 request to send
		GPIO10	36			
		GPIO27	18	VIO2		
		GPIO32	12			
	UART2_CTS	GPIO6	41	VIO1	I	UART2 clear to send
		GPIO11	35			
		GPIO28	17	VIO2		
		GPIO33	11			

(1) Drive strength for GPIO's can be user defined.

4. Electrical Specifications

4.1. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

Table 4. Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
VDD_3V3	VDD_3V3 supply	–0.5	4.2	V
VDD_1V8	VDD_1V8 supply	–0.5	2.1	V
VIO1, VIO2	VDD IO Voltage	–0.5	3.6	V
	Input Voltage to all digital pins	–0.5	V_{IO} + 0.5	V
T_A	Operating Ambient Temperature	–40	105	°C
T_{stg}	Storage temperature	–55	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

4.2. ESD Ratings

Table 5. ESD Ratings

PARAMETER	DESCRIPTION	VALUE	UNIT	NOTE
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

4.3. Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Table 6. Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
VDD_1V8	VDD_18V supply	1.71	1.8	1.98	V
VDD_3V3	VDD_3V3 supply	3	3.3	3.6	
VIO1, VIO2, VDD_SF (1)(2)	DC supply rail for input/output	1.71/3	1.8/3.3	1.98/3.6	
T_A	Operating ambient temperature	–40		85	°C
	Maximum power dissipation			2	W

(1) VIO1 and VIO2 pins can be set to either 1.8 or 3.3 V.

(2) VIO2 and VDD_SF must be set to 1.8V for PSRAM variants.

(3) VDD_SF should be set to 1.8V by default, otherwise noted.

4.4. GPIO Characteristics

Table 7. GPIO Characteristics

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
GPIO pullup current	Input mode, pullup enabled, Vpad = 0V	VIO = 1.8V	9	20	42	µA
		VIO = 3.3V	45	86	155	
GPIO pulldown current	Input mode, pullup enabled, Vpad = 0V	VIO = 1.8V	9	20	43	
		VIO = 3.3V	39	80	151	
V_{IH}	High Level Input Voltage		0.7 x V_{IO}		V_{IO}	V
V_{IL}	Low Level Input Voltage		0		0.3 x V_{IO}	
V_{OH}	High Level Output Voltage	at 4mA	V_{IO} – 0.4		V_{IO}	
V_{OL}	Low Level Output Voltage	at 4mA(1)	0		0.4	

(1) Low drive GPIO in low drive mode tested at 2mA.

4.5. Power Consumption

4.5.1. Current Consumption - 2.4GHz WLAN Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

Table 8. Current Consumption - 2.4GHz WLAN Static Modes

PARAMETER	TEST CONDITIONS		VDD_1V8		VDD_3V3		UNIT
			TYP	MAX	TYP	MAX	
TX (Continuous)(1)	1 DSSS	TX Power = 18.5 dBm	120	195	310	335	mA
	6 OFDM	TX Power = 18.2 dBm	134	210	298	342	
	54 OFDM	TX Power = 15.9 dBm	141		242		
	HT MCS0	TX Power = 18.3 dBm	136		305		
	HT MCS7	TX Power = 15.8 dBm	141		242		
	HE MCS0	TX Power = 18.2 dBm	134		304		
	HE MCS7	TX Power = 15.7 dBm	139		240		
RX	Continuous Listen (for Beacon)		60		0		mA
	Active RX		64		0.4		

(1) Peak current VDD_3V3 can reach up to 495mA during device calibration. Peak current VDD_1V8 is 400mA including peripherals and internal cortex

4.5.2. Current Consumption - 5GHz WLAN Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

Table 9. Current Consumption - 5GHz WLAN Static Modes

PARAMETER	TEST CONDITIONS		VDD_1V8		VDD_3V3		UNIT
			TYP	MAX	TYP	MAX	
TX (Continuous)(1)	6 OFDM	TX Power = 19.6 dBm	193	275	295	348	mA
	54 OFDM	TX Power = 15.3 dBm	196		224		
	HT MCS0	TX Power = 19.7 dBm	195		305		
	HT MCS7	TX Power = 15.2 dBm	196		224		

Table 9. Current Consumption - 5GHz WLAN Static Modes (continued)

PARAMETER	TEST CONDITIONS		VDD_1V8		VDD_3V3		UNIT
			TYP	MAX	TYP	MAX	
	HE MCS0	TX Power = 19.7 dBm	193		302		
	HE MCS7	TX Power = 14.1 dBm	194		214		
RX	Continuous Listen (for Beacon)		96		0		mA
	Active RX		117		0.4		

(1) Peak current VDD_3V3 can reach up to 495mA during device calibration. Peak current VDD_1V8 is 400mA including peripherals and internal cortex.

4.5.3. Current Consumption - Bluetooth LE Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

Table 10. Current Consumption - Bluetooth LE Static Modes

PARAMETER	TEST CONDITIONS	VDD_1V8		VDD_3V3		UNIT
		TYP	MAX	TYP	MAX	
TX (Continuous)	TX Power = 0dBm	110		58		mA
	TX Power = 10dBm	111		135		
	TX Power = 20dBm	113		315		
RX		64		0.4		

4.5.4. Current Consumption - MCU Modes

Table 11. Current Consumption - MCU Modes

PARAMETER		TEST CONDITIONS	VDD_1V8	VDD_3V3	UNIT
			TYP	TYP	
Host MCU Active, Wireless Core Sleep	Host MCU 160MHz running, Wi-Fi/Bluetooth LE Core sleep		22		mA

Table 11. Current Consumption - MCU Modes (continued)

PARAMETER		TEST CONDITIONS	VDD_1V8	VDD_3V3	UNIT
			TYP	TYP	
Host MCU Shutdown		External supplies are available, device held in reset (nReset is low)	14	4	µA

4.6. Timing and Switching Characteristics

4.6.1. Clock Specifications

The module series uses two clocks for operation:

- An on-board fast clock running at 52 MHz for active MCU functions and peripherals, as well as WLAN/ Bluetooth LE.
- A slow clock running at 32.768 kHz for low power modes. The slow clock can be generated internally or externally. The LFXT or the oscillator is not included in the module.

4.6.1.1. HFXT Characteristics

The module series uses a 52MHz crystal oscillator. The characteristics of this crystal is as below table.

Table 12. HFXT Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			52		MHz
Frequency accuracy	Initial + temperature + aging	-20		+20	ppm
Load Capacitance, C_L			8		pF
Equivalent series resistance, ESR			20		Ω

4.6.1.2. Slow Clock Requirements

In order to minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and consumes more power than sourcing the slow clock externally. For this scenario the SLOW_CLK_IN pin should be left not connected.

For optimal power consumption, the slow clock can be generated externally by an oscillator, XTAL, or sourced from elsewhere in the system. If using an oscillator, the external source must meet the requirements listed below. This clock should be fed into the module pin Slow_CLK_IN/GPIO0 and should be stable before nReset is deasserted and device is enabled. The clock signal logic high should be the same voltage as VIO1 IO Ring.

Table 13. External Slow Clock Oscillator Requirements

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
	Input slow clock frequency	Square wave		32.768		kHz
	Frequency accuracy	Inital + temperature + aging	-250		+250	ppm
	Input Duty cycle		30	50	70	%
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
	Input impedence		1			MΩ
	Input capacitance				5	pF

If using an XTAL, the external source must meet the requirements listed below. The crystal pins should be fed into the module pins LFXT_P/GPIO0 and LFXT_N/GPIO1.

Table 14. External Slow Clock XTAL Requirements

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			32.768		kHz
Frequency accuracy	Initial + temperature + aging	-250		+250	ppm
Load Capacitance, C_L (1)		3		12.5	pF
Equivalent series resistance, ESR				100	kΩ

(1) Load capacitance, $C_L = [C1*C2] / [C1 + C2] + C_P$, where C1, C2 are the capacitors connected on LFXT_P and LFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.

4.6.2. Peripheral Characteristics

4.6.2.1. ADC

The module series supports eight ADC channels, 12-bit, with the following specifications.

Over operating free-air temperature range (unless otherwise noted).

Table 15. ADC Electrical Specifications

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions					

Table 15. ADC Electrical Specifications (continued)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins, VIO1 = 3.3V	0		3.2	V
		All ADC analog input pins, VIO1 = 1.8V	0		1.8	
V_{R+}	Positive ADC reference voltage	ADC reference sourced from external reference pin (VeREF+)		1.8		V
ADC Switching Characteristics						
F_S ADCREF	ADC sampling frequency when using the internal ADC reference voltage				1	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage				2	Msps
ADC Linearity Parameters						
E_I	Integral linearity error (INL)		-2	+/-1	2	LSB
E_D	Differential linearity error (DNL)		-1	+/-0.5	1	LSB
E_O	Offset error - even channel		-3	+/-2	3	LSB
E_G	Gain error		-100	+/-3	100	LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits			11		bit
SINAD	Signal-to-noise and distortion ratio	External Reference		66		dB
		Internal Reference		63		

4.6.2.2. I2C

The I^2C timing parameters are shown as below table.

Over operating free-air temperature range (unless otherwise noted)

Table 16. I^2C Timing Parameters

ARAMETERS		STANDARD MODE		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0.1		0.4		1	MHz

Table 16. I^2C Timing Parameters (continued)

ARAMETERS		STANDARD MODE		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{HD,STA}$	Hold time (repeated) START	4		0.6		0.26		μs
t_{LOW}	LOW period of the SCL clock	4.7		1.3		0.5		μs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		μs
$t_{SU,STA}$	Setup time for a repeated START	4.7		0.6		0.26		μs
$t_{HD,DAT}$	Data hold time	0		0		0		μs
$t_{SU,DAT}$	Data setup time	250		100		50		μs
$t_{SU,STO}$	Setup time for STOP	4		0.6		0.26		μs
t_{buf}	bus free time between a STOP and START condition	4.7		1.3		0.5		μs
$t_{VD,DAT}$	data valid time		3.45		0.9		0.45	μs
$t_{VD,ACK}$	data valid acknowledge time		3.45		0.9		0.45	μs

The I^2C timing diagram is shown as below figure.

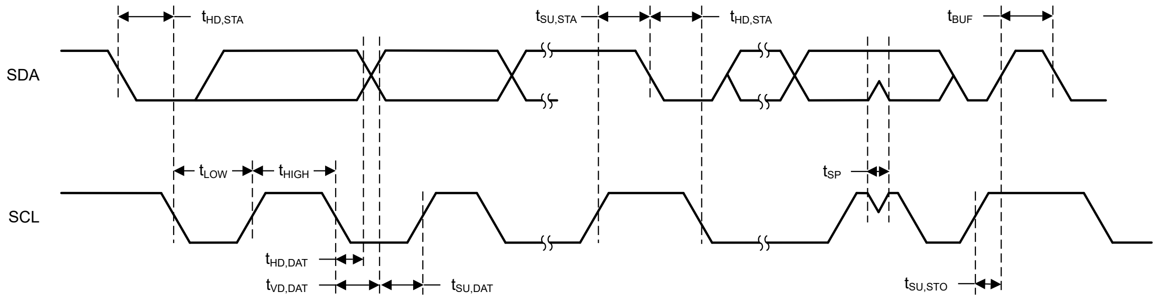


Figure 6. I2C Timing Diagram

4.6.2.3. SPI

The timing parameters of SPI controller mode are shown as below table.

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted).

Table 17. SPI Timing Parameters - Controller Mode

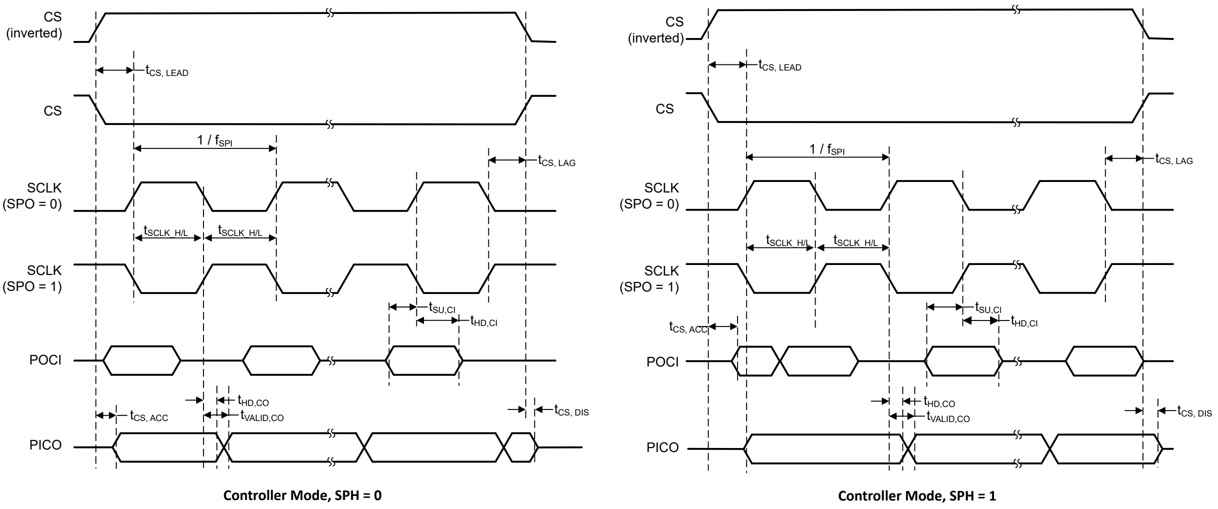
PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	SPI clock frequency	Controller Mode			40	MHz
DC_{SCLK}	SCLK Duty Cycle		47.5	50	52.5	%
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 0, National Semiconductor (Microwire)	1			SCLK
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 1	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 0, National Semiconductor (Microwire)	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 1	1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{SU.CI}$	POCI input data setup time(3)		15.9			ns
$t_{HD.CI}$	POCI input data hold time		0			ns
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid, C_L = 20pF			2.2	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge.

(2) Specifies how long data on the output is valid after the output changing SCLK clock edge.

(3) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.

The timing diagram of SPI controller mode is shown as below figure.



Controller Mode, SPH = 0

Controller Mode, SPH = 1

Figure 7. SPI Timing Diagrams - Controller Mode

The timing parameters of SPI peripheral mode are shown as below table.

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted).

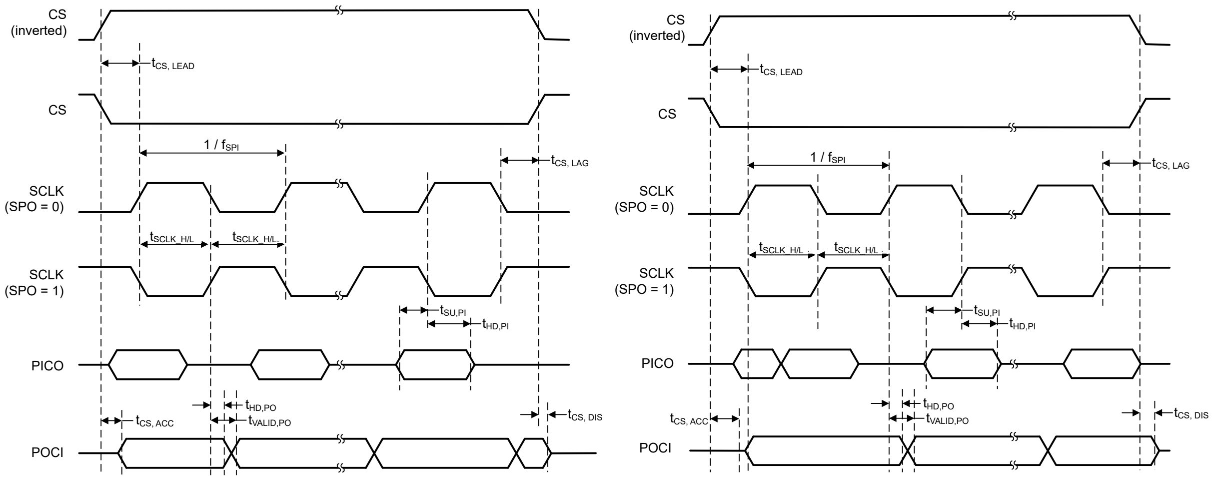
Table 18. SPI Timing Parameters - Peripheral Mode

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	SPI clock frequency	Peripheral Mode			30	MHz
DC_{SCLK}	SCLK Duty Cycle		45	50	55	%
t-CS.LEAD	CS lead-time, CS active to clock	Motorola Clock Phase 0, National Semiconductor (Microwire)	1			SCLK
t-CS.LEAD	CS lead-time, CS active to clock	Motorola Clock Phase 1	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 0, National Semiconductor (Microwire)	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 1	1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out				15	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				15	ns
$t_{SU.PI}$	PICO input data setup time		2.8			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
t-VALID.PO	POCI output data valid time(1)	SCLK edge to POCI valid, C_L = 20pF			10.2	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge.

(2) Specifies how long data on the output is valid after the output changing SCLK clock edge.

The timing diagram of SPI peripheral mode is shown as below figure.



Peripheral Mode, SPH = 0

Peripheral Mode, SPH = 1

Figure 8. SPI Timing Diagrams - Peripheral Mode

4.6.2.4. xSPI

The module series uses an external serial flash for application code. The interface to the flash is with Quad SPI (QSPI) interface.

The QSPI timing parameter are shown as below table.

Table 19. QSPI Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Q_{CLK}	QSPI Clock frequency, CLK		80	MHz

4.6.2.5. UART

The UART timing parameters are shown as below table.

Table 20. UART Timing Parameters

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud rate		37.5		4364	kbps

4.6.2.6. I2S

The timing parameters of I^{2}S controller mode are shown as below table.

Table 21. I^{2}S Timing Parameters - Controller Mode

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	clock frequency, BCLK	Controller Mode			3.072	MHz
DC_{SCLK}	Clock Duty Cycle		40	50	60	%
$t_{SDIN.setup}$	SD data input setup time (before rising edge of SCLK)		9			ns
$t_{SDIN.hold}$	SD data input hold time (after rising edge of SCLK)		5			ns
$t_{WS.valid}$	WS data output valid time (Falling edge of SCLK to WS data valid)		42		49	ns
$t_{SD\text{-}OUT.valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		37		62	ns

The timing parameters of I^{2}S peripheral mode are shown as below table.

Table 22. I^{2}S Timing Parameters - Peripheral Mode

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	clock frequency, BCLK	Peripheral Mode			3.072	MHz
DC_{SCLK}	Clock Duty Cycle		40	50	60	%
$t_{SDIN.setup}$	SD data input setup time (before rising edge of SCLK)		9			ns
$t_{SDIN.hold}$	SD data input hold time (after rising edge of SCLK)		5			ns
$t_{WS.setup}$	WS data input setup time (before rising edge of SCLK)		15			ns
$t_{WS.hold}$	WS data input hold time (after rising edge of SCLK)		0			ns
$t_{SD\text{-}OUT.valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		26		47	ns

4.6.2.7. PDM

The PDM timing parameters are shown as below table.

Table 23. PDM Timing Parameters

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	PDM clock output Frequency		0.016		6.144	MHz

Table 23. PDM Timing Parameters (continued)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tr	PDM Clock Rise time				5	ns
t_{DC}	PDM Clock duty Cycle		40	50	60	%
t_{delay}	Decimation filter Delay				5	ms
t_{is}	Left/Right Data Setup Time	Left/Right	20			ns
t_{ih}	Left/Right Data Hold Time	Left/Right	0			ns

4.6.2.8. CAN

The CAN characteristics are shown as below table.

Table 24. CAN Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CAN_TX_LOAD	DCAN TX load capacitance		4	10	pF
CAN_RX_t_RCAN_RX_t_F	DCAN RX rise and fall times		10	75	ns
$t_{p(CAN\_TX)}$	Propagation delay	Transmit shift register to CAN_TX pin		10	ns
$t_{p(CAN\_RX)}$	Propagation delay	CAN_RX pin to receive shift register		5	ns

4.6.2.9. SDMMC

The timing parameters of SDMMC in default speed are shown as below table.

Table 25. SDMMC Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		20	MHz
DC_{clock}	Clock Duty cycle	47.5	52.5	%
t_{TLH}	Rise time, CLK		3	ns
t_{THL}	Fall time, CLK		3	ns
t_{ISU}	Setup time, input valid before CLK ↑	2.5		ns
t_{IH}	Hold time, input valid after CLK ↑	0		ns
t_{ODLY}	Delay time, CLK ↓ to output valid	0	4	ns
C_L	Capacitive load on outputs		35	pF

The timing parameters of SDMMC in high speed are shown as below table.

Table 26. SDMMC Timing Parameters - High Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		40	MHz
DC_{clock}	Clock Duty cycle	47.5	52.5	%
t_{TLH}	Rise time, CLK		3	ns
t_{THL}	Fall time, CLK		3	ns
t_{ISU}	Setup time, input valid before CLK ↑	2.5		ns
t_{IH}	Hold time, input valid after CLK ↑	2.15		ns
t_{ODLY}	Delay time, CLK ↑ to output valid	0	4	ns
C_L	Capacitive load on outputs		35	pF

4.6.2.10. SDIO

The timing parameters of SDIO in default speed are shown as below table.

Table 27. SDIO Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		26	MHz
t_{WH}	High Period	10		ns
t_{WL}	Low Period	10		
t_{TLH}	Rise time, CLK		10	
t_{THL}	Fall time, CLK		10	
t_{ISU}	Setup time, input valid before CLK ↑	5		
t_{IH}	Hold time, input valid after CLK ↑	5		
t_{ODLY}	Delay time, CLK ↓ to output valid. *15pF (Min); 40pF (Max)	2.5	14	
C_L	Capacitive load on outputs		40	pF

The timing diagram of SDIO in default speed are shown as below figure.

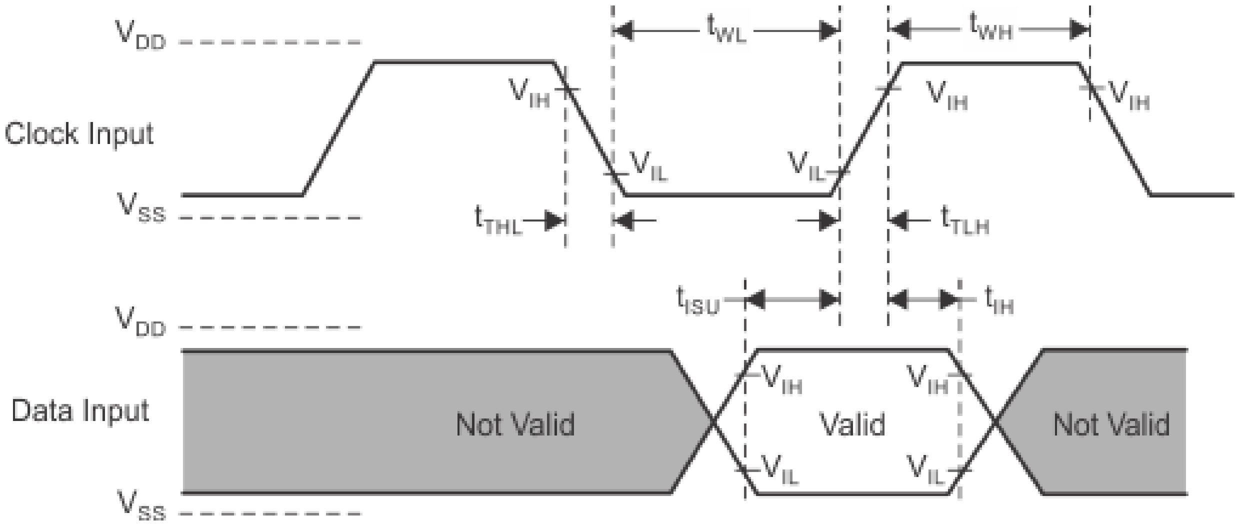


Figure 9. SDIO Default Input Timing

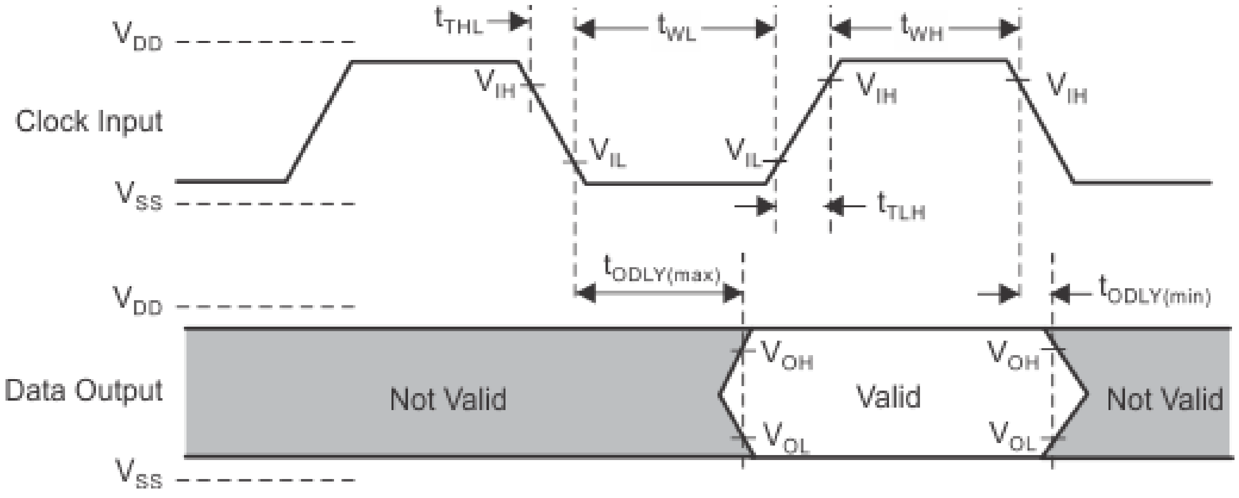


Figure 10. SDIO Default Output Timing

The timing parameters of SDIO in high speed are shown as below table.

Table 28. SDIO Timing Parameters - High Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		52	MHz
t_{WH}	High Period	7		ns
t_{WL}	Low Period	7		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{ISU}	Setup time, input valid before CLK ↑	6		

Table 28. SDIO Timing Parameters - High Speed (continued)

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↑ to output valid. *15pF (Min); 40pF (Max)	2.5	14	
C_L	Capacitive load on outputs		40	pF

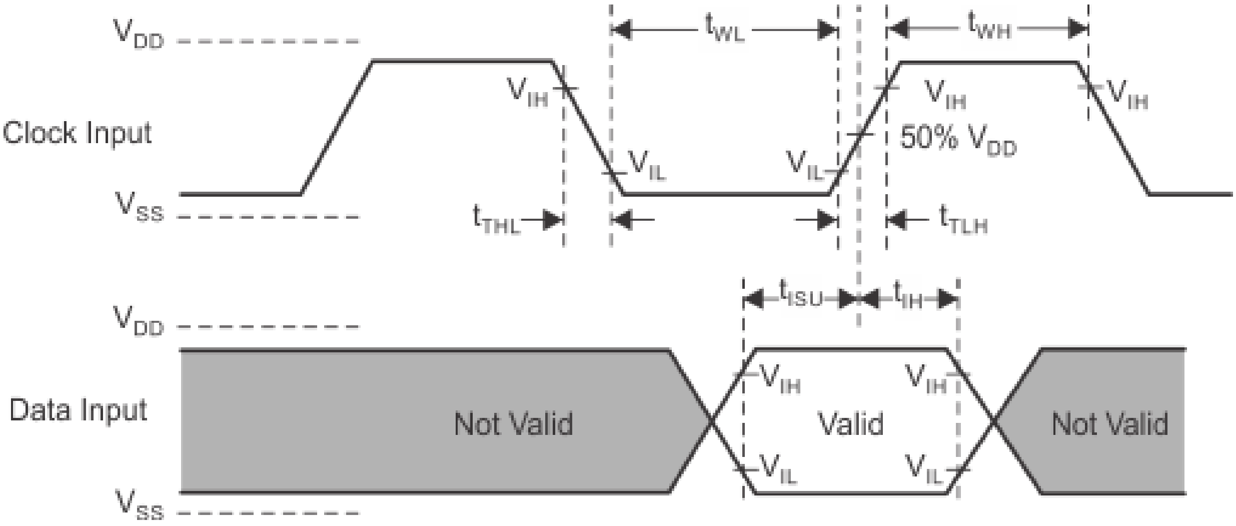


Figure 11. SDIO High Speed Input Timing

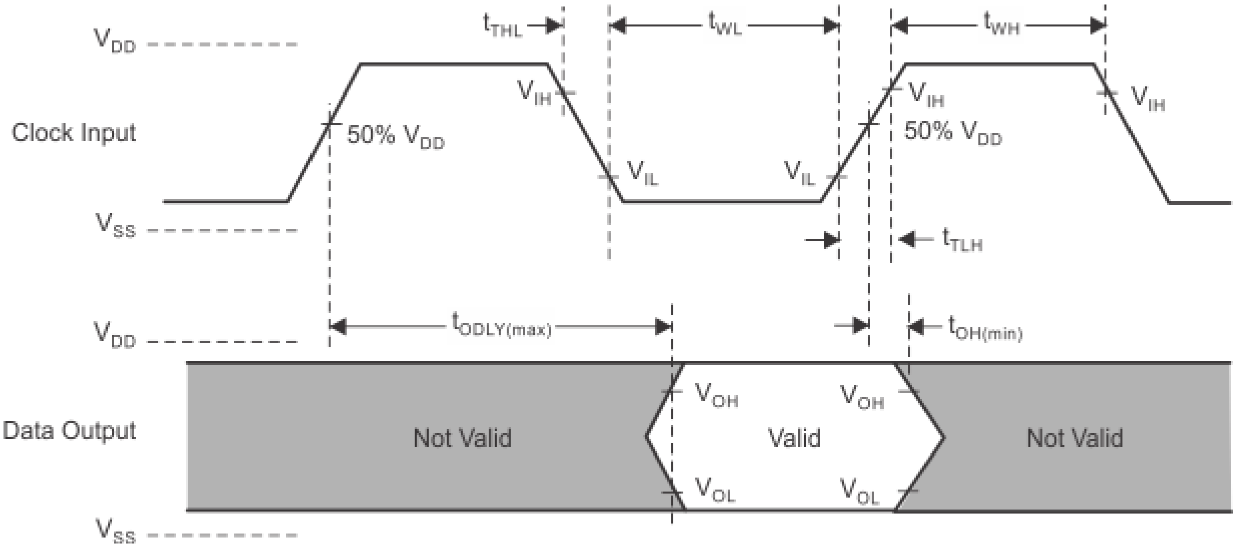


Figure 12. SDIO High Speed Output Timing

4.7. Radio Specifications

4.7.1. WLAN Performance: 2.4-GHz Receiver Characteristics

Table 29. WLAN Performance: 2.4-GHz Receiver Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHz
Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 Mbps DSSS		-96.5		dBm
	2 Mbps DSSS		-94		
	11 Mbps CCK		-89		
	6 Mbps OFDM		-91.5		
	54 Mbps OFDM		-74		
	HT MCS0 MM 4K		-91.5		
	HT MCS7 MM 4K		-72		
	HE MCS0 4K		-89		
	HE MCS7 4K		-70		

(1) The typical value is the average across all channels.

4.7.2. WLAN Performance: 2.4-GHz Transmitter Power

Table 30. WLAN Performance: 2.4-GHz Transmitter Power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHz
Maximum output power at VDD_3V3 = 3.3V	1 Mbps DSSS		18.5		dBm
	6 Mbps OFDM		18.2		
	54 Mbps OFDM		15.9		
	HT MCS0 MM		18.3		
	HT MCS7 MM		15.8		
	HE MCS0		18.2		
	HE MCS7		15.7		

(1) The typical value is the average across all channels.

4.7.3. WLAN Performance: 5-GHz Receiver Characteristics

Table 31. WLAN Performance: 5-GHz Receiver Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		5180		5845	MHz
Sensitivity (10% PER for 11a/n/ax rates)	6Mbps OFDM		-91.5		dBm
	54Mbps OFDM		-75.5		
	HT MCS0 MM 4K		-93		
	HT MCS7 MM 4K		-73.5		
	HE MCS0 4K		-91.5		
	HE MCS7 4K		-71.5		

(1) The typical value is the average across all channels.

4.7.4. WLAN Performance: 5-GHz Transmitter Power

Table 32. WLAN Performance: 5-GHz Transmitter Power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		5180		5845	MHz
Maximum output power at VDD_3V3 = 3.3V	6 Mbps OFDM		19.6		dBm
	54 Mbps OFDM		15.3		
	HT MCS0 MM		19.7		
	HT MCS7 MM		15.2		
	HE MCS0 20 MHz		19.7		
	HE MCS7 20 MHz		14.1		

(1) The typical value is the average across all channels

4.7.5. Bluetooth LE Performance: Receiver Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Bluetooth LE 125Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.2%		-103.5		dBm
Bluetooth LE 500Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.2%		-101		dBm
Bluetooth LE 1Mbps (LE 1M) Receiver Characteristics					
Receiver sensitivity	PER <30.2%, 37-byte packets		-97.5		dBm
Receiver sensitivity	PER <30.2%, 255 byte-packets		-96.5		dBm
Bluetooth LE 2Mbps (LE 2M) Receiver Characteristics					
Receiver sensitivity(2)	PER <30.2%		-95.5		dBm

(1) The typical value is the average across all channels. The RX sensitivity on channel 19 might degrade by up to 2dB for 125Kbps PHY and 1.5dB for 500kbps PHY.

4.7.6. Bluetooth LE Performance - Transmitter Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Output Power	Highest setting - 20 dBm setting		16.3		dBm

(1) The typical value is the average across all channels.

4.8. Antenna Specifications

TBD.

5. Mechanical Specifications

5.1. Module Dimensions

The module dimensions are shown as following figures. All dimensions are in mm.

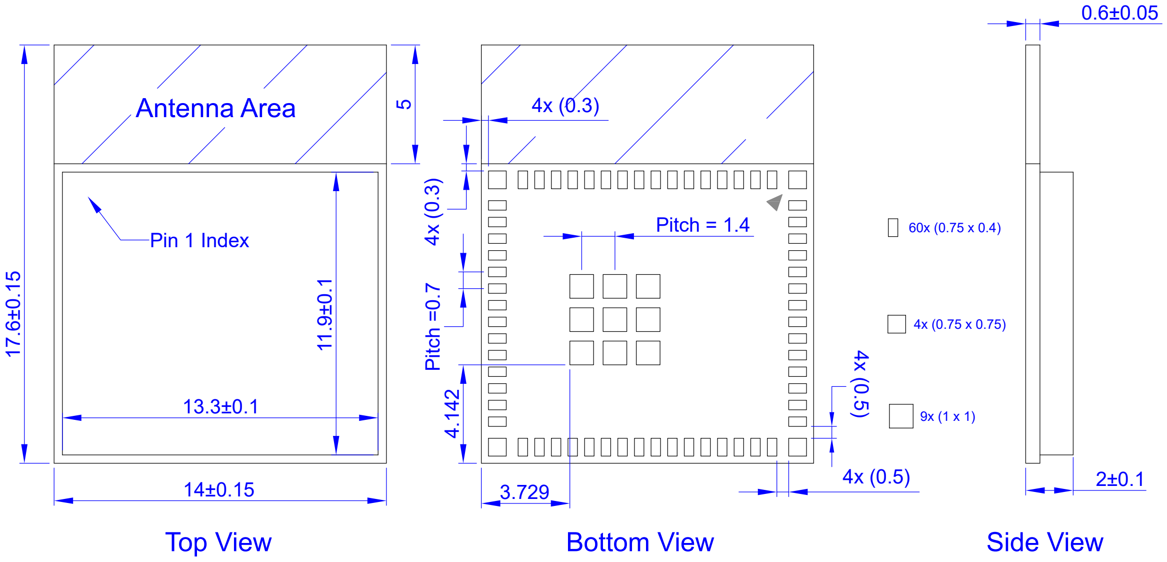


Figure 13. Mechanical Drawing of BDE-BW3551A

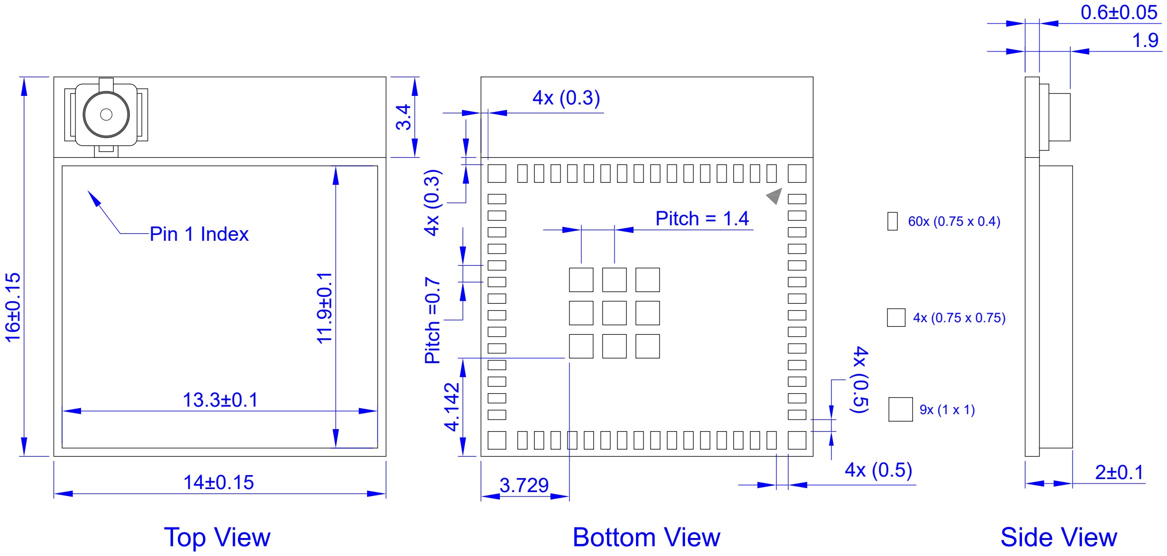


Figure 14. Mechanical Drawing of BDE-BW3551U

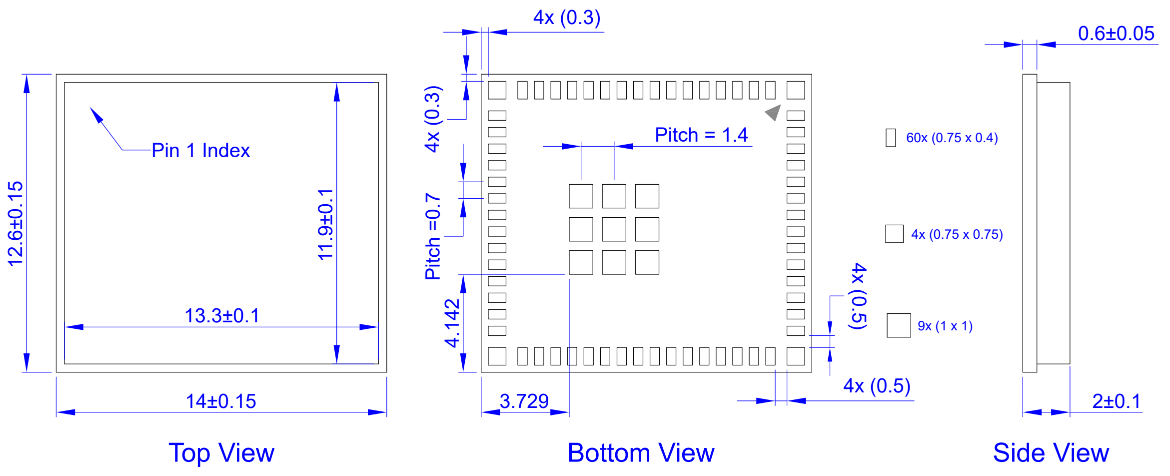


Figure 15. Mechanical Drawing of BDE-BW3551N

5.2. PCB Footprint

The recommended PCB footprints for the module series are as below figure. All dimensions are in mm.

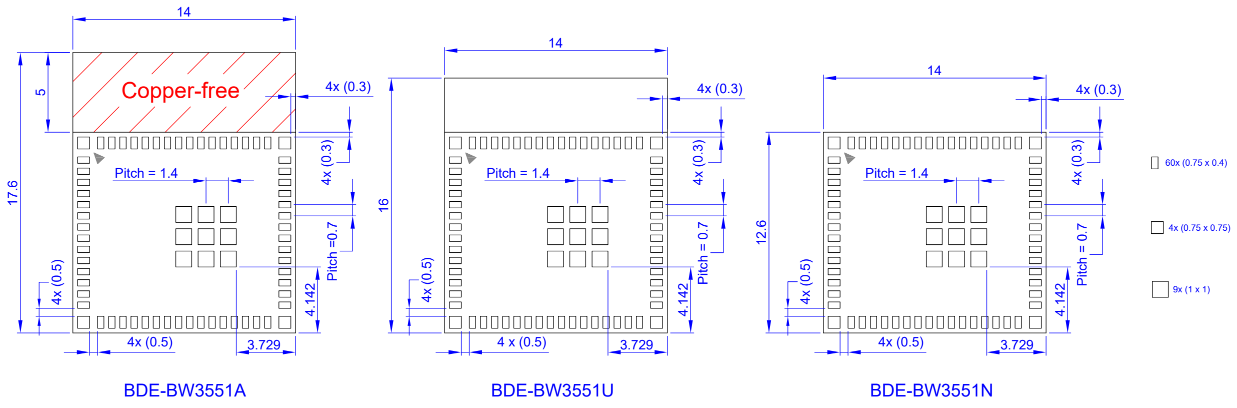


Figure 16. Recommended PCB Footprints

(1) Solder mask should be the same or 5% larger than the dimension of the pad.

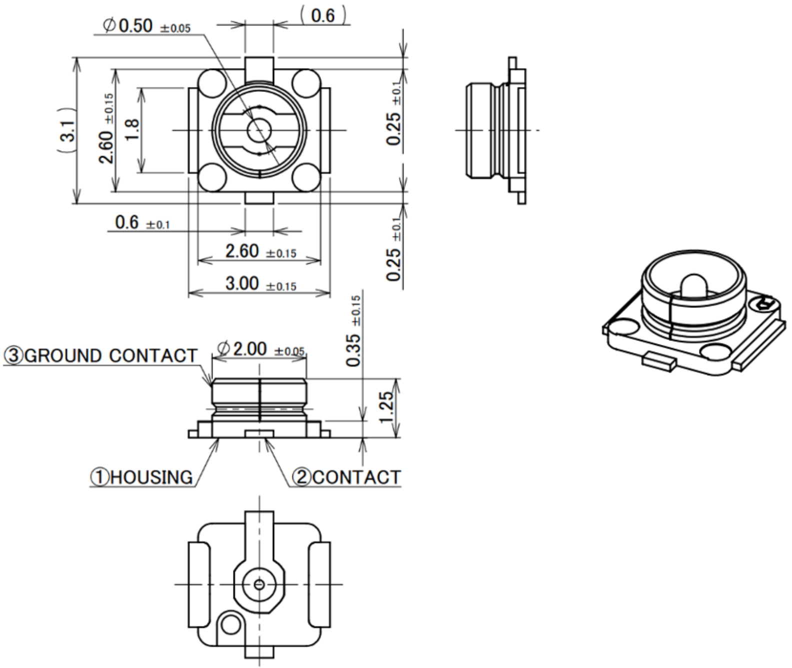
(2) Solder paste must be the same as the pin for all peripheral pads. For thermal pads, make the solder paste 20% smaller than the pad.

(3) Copper-free means no copper in this area in all layers, including traces, ground or components etc. It is recommended to extend the copper-free area at least 15mm to the left and right. For U.FL variants, ground pour can be applied but avoid signal lines underneath this area.

(4) Customers can modify the land pattern dimensions based on their manufacturing experience.

5.3. U.FL Connector

The specifications of the U.FL connector assembled on the module are as below figure. All dimensions are in mm.



RATING VOLTAGE	60 V AC (R.M.S)	
RATING FREQUENCY	DC～9GHz	
OPERATING TEMPERATURE	233～363K (−40℃～+90℃)	
VSWR	RECEPTACLE: 1.3 MAX. AT 0.1～3 GHz, 1.4 MAX. AT 3～6 GHz, 1.8 MAX. AT 6～9 GHz	
MAIN CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 20 mohm MAX.	
GROUND CONTACT RESISTANCE	INITIAL: 20 mohm MAX. / AFTER TEST: ⊿R 100 mohm MAX.	
INSULATION RESISTANCE	INITIAL: 500 Mohm MIN. / AFTER TEST: 100 Mohm MIN.	
DIELECTRIC WITHSTANDING VOLTAGE	200 V AC, 1 MINUTE	
DURABILITY	30 CYCLES	
UNMATING FORCE (INITIAL / AFTER TEST)	INITIAL: 5 N MIN. AFTER TEST: 3 N MIN.	INITIAL: 4 N MIN. AFTER TEST: 2 N MIN.

Figure 17. U.FL Connector Specifications

6. Integration Guideline

6.1. System Diagram

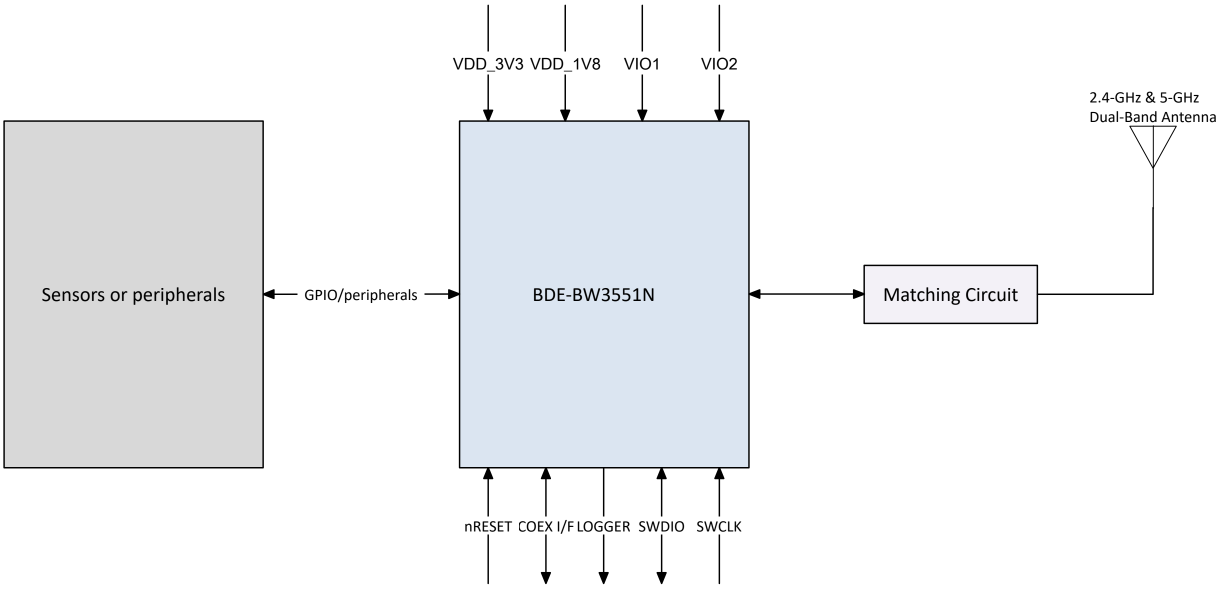


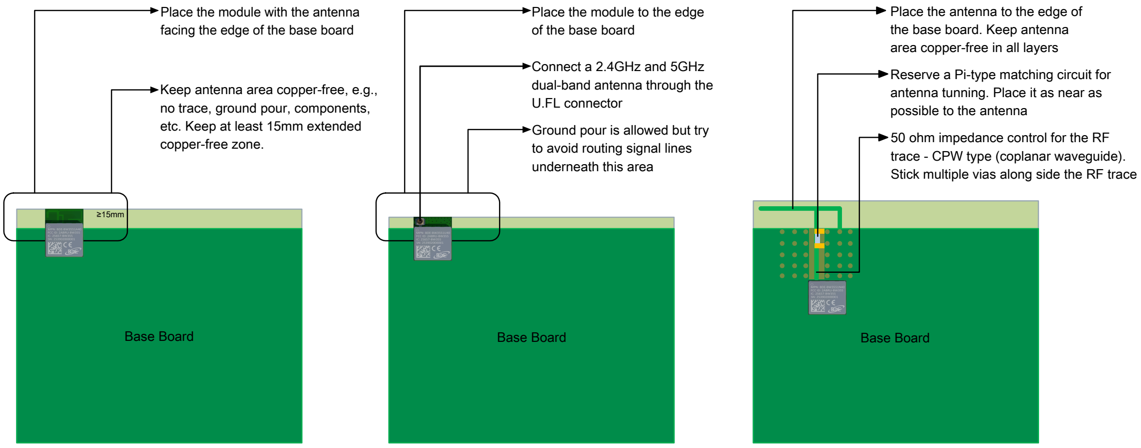
Figure 18. High-Level System Block Diagram

(1) Proper decoupling capacitors are recommended to be placed close to the power pins of the module.
(2) VIO1 and VIO2 should be set to 3.3V or 1.8V depending on the system voltage. VIO2 can only be set to 1.8V if PSRAM variants are used.
(3) Pull-up resistor, e.g. 100K ohm, is required to be placed to nRESET line.
(4) LOGGER are sensed by the device during boot, with boot value to be "1", which is LOGGER pin being pulled up.
(5) SWDIO and SWCLK is for SWD debug, recommended to be exposed to the test points or headers.
(6) LOGGER is for logs output, recommended to be exposed to a test point or hearer.
(7) COEX I/F is the coexistence interface, mutiplexed with GPIOs.
(8) For PCB trace antenna variants, the external antenna and its matching circuit are not needed.
(9) For U.FL varants, the antenna is connected through U.FL connector.

6.2. Module Placement

The placement of the module in the base board is critical in your design. Improper placement can lead to poor antenna performance. BDE recommends following below practical placement to achieve expected antenna performance.

Any form of proximity to the metal or other material will change/degrade the antenna performance. Keep the antenna area as far as possible to the metal material in any direction. If metal materials cannot be avoided in your design, for example the design with metal enclosure, we recommend keep the antenna area at least 40mm distance to the enclosure in all directions. Customers should verify the communication range with the mock-up or real product prototype on their own.



Place the module with the antenna facing the edge of the base board

Keep antenna area copper-free, e.g., no trace, ground pour, components, etc. Keep at least 15mm extended copper-free zone.

Place the module to the edge of the base board

Connect a 2.4GHz and 5GHz dual-band antenna through the U.FL connector

Ground pour is allowed but try to avoid routing signal lines underneath this area

Place the antenna to the edge of the base board. Keep antenna area copper-free in all layers

Reserve a Pi-type matching circuit for antenna tunning. Place it as near as possible to the antenna

50 ohm impedance control for the RF trace - CPW type (coplanar waveguide). Stick multiple vias along side the RF trace

Figure 19. Recommended Module Placement

6.3. General Design Considerations

Table 33. General Design Considerations

Thermal	
1	The proximity of ground vias must be close to each ground pad of the module.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.

Table 33. General Design Considerations (continued)

10	RF traces must have constant impedance (50-ohm Coplanar or microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
14	BDE recommends using double-shielded coaxial RF cable to connect with the U.FL connector with antenna if the U.FL variants are selected.
15	Do not place or run the RF cable right above or below the module.
16	If there are some other radios besides this module in the system, try to place them apart as far as possible. And ensure there is at least 25 dB isolation between the antenna port of every radio.
Supply and Interface	
17	The power trace for VDD_3V3 is recommended to be at least 20-mil wide.
18	The VDD_1V8 trace is recommended to be at least 20-mil wide.
19	Make VDD_3V3 and VDD_1V8 traces as wide as possible to ensure reduced inductance and trace resistance.
20	If possible, shield VDD_3V3 and VDD_1V8 traces with ground above, below, and besides the traces.
21	SDIO/SDMMC signals traces must be routed in parallel to each other and as short as possible (less than 12cm).In addition, every trace length must be the same as the others. There should be enough space between traces-greater than 1.5 times the trace width to ensure signal quality, especially for the CLK trace. Remember to keep these traces away from the other digital or analog signal traces. It is recommended adding ground shielding around these buses.
22	SDIO/SDMMC and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

6.4. Development Resources

Each module will have a breakout board for its own and it can be interfaced with the plug-in evaluation module BDE-LPEM.

For more information on the development kits, please visit the product page on bdecomm.com or refer to the **Module User Guide**.

7. Handling Instructions

The module is the surface mount module with LGA footprint. It is designed to conform to the major manufacturing guidelines, including the commercial, industrial manufacturing process.

In this section, we will cover the basic shipping information, including the module markings, packaging, labeling, etc. And also, the instructions on how to handle the module in terms of storage, assembly and so on.

7.1. Module Marking

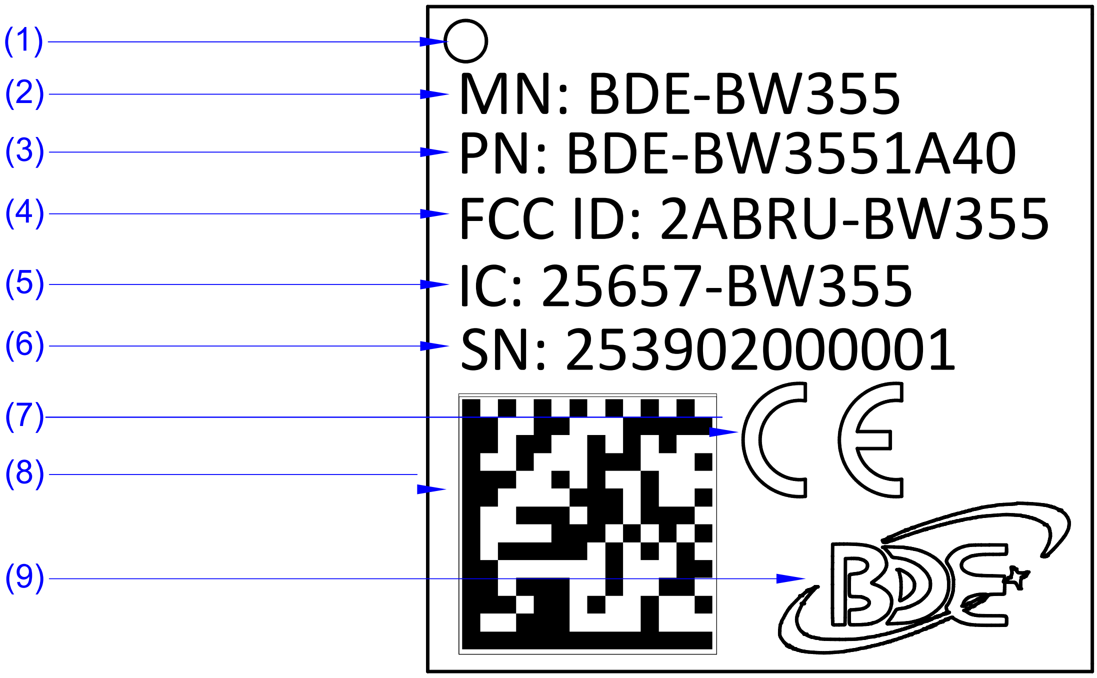


Figure 20. Module Marking

(1) Pin one indicator.
(2) Model number;
(3) Part number or orderable part number.
(4) FCC ID.
(5) IC number.
(6) Serial number for traceability.
(7) CE mark.
(8) Data matrix code for SN.
(9) BDE logo.

7.2. Packing Information

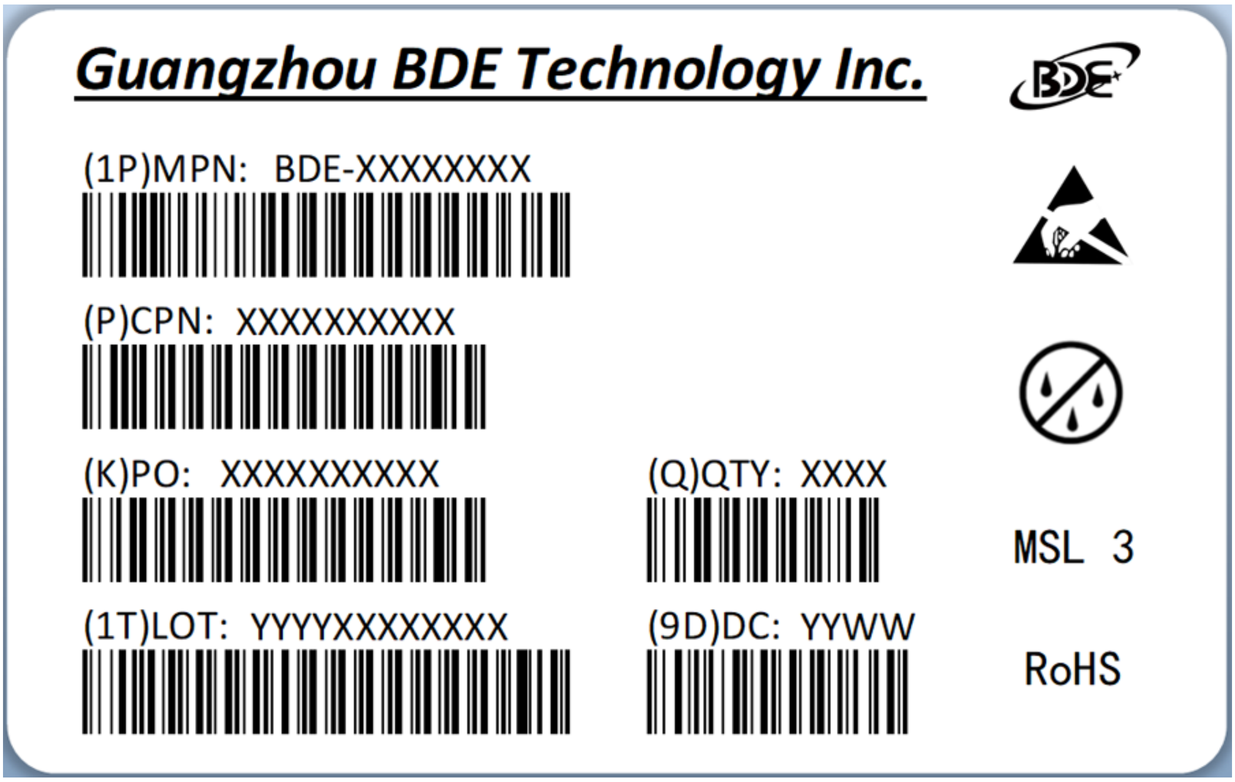
7.2.1. Tape & Reel Information

TBD.

7.2.2. Labeling

7.2.2.1. Reel Label Information

The reel label will be affixed onto the reel, Anti-ESD bag and reel box. It mainly shows the MPN (Manufacturer Part Number), CPN (Customer Part Number), PO (Purchase Order Number), LOT number, QTY (Quantity), DC (Date Code) and MSL (Moisture Sensitivity Level). Sometimes, it also shows other information, such as the regulatory information.



Guangzhou BDE Technology Inc.

(1P)MPN: BDE-XXXXXXXX

(P)CPN: XXXXXXXXXX

(K)PO: XXXXXXXXXX

(Q)QTY: XXXX

(1T)LOT: YYYYXXXXXXX

(9D)DC: YYWW

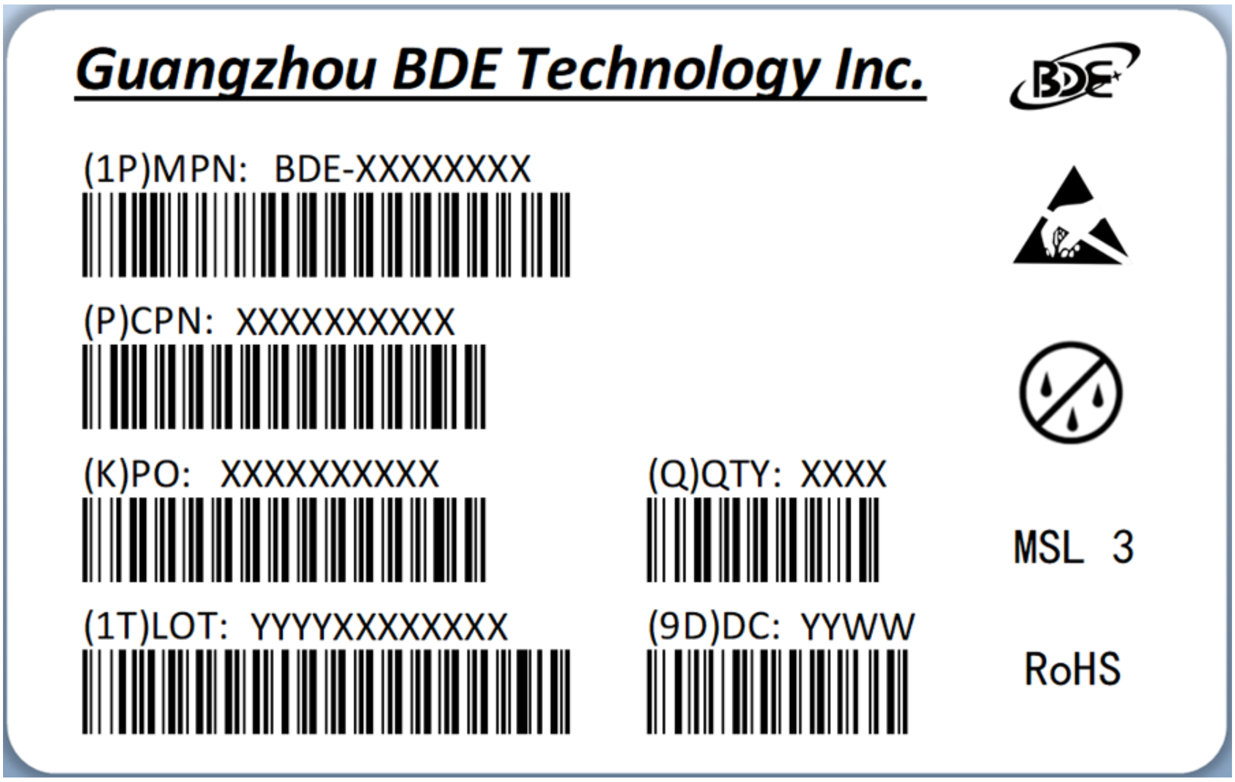
MSL 3

RoHS

Figure 21. Reel Label Information

7.2.2.2. Carton Label Information

The carton label will be affixed onto the surface of the carton. If the carton contains different Part Numbers or POs, there will be different labels representing different Part Numbers, different POs and Quantity.



Guangzhou BDE Technology Inc.

(1P)MPN: BDE-XXXXXXXX

(P)CPN: XXXXXXXXXX

(K)PO: XXXXXXXXXX

(Q)QTY: XXXX

(1T)LOT: YYYYXXXXXXXX

(9D)DC: YYWW

MSL 3

RoHS

Figure 22. Carton Label 1 Information

Guangzhou BDE Technology Inc.

CTN : X of Y

SHIP DATE: YYYY/MM/DD

G.W. : XX KG

Made in China

Figure 23. Carton Label 2 Information

7.2.3. Carton Information

TBD.

7.3. Assembly Instructions

7.3.1. Moisture Sensitive Level

The MSL (Moisture Sensitive Level) of the module is MSL-3. Handling guidelines are listed as below:

1. The floor life for MSL-3 device is 168 hours in ambient environment 30°C/60%RH. Before assembly, make sure to check if the modules are packaged with desiccate and humidity indicator card;
2. After the bag is opened, make sure to mount the modules within 168 hours at factory conditions (< 30°C/60% RH) or stored at <10% RH. Repackage is needed with new desiccate and humidity indicator card if the modules are not mounted before exceeding floor life;
3. If the card reads >10%, or the modules have been exposed for over 168 hours, the modules need to be baked before mounted. Recommended baking condition is 125°C for 8 hours.

7.3.2. Reflow Profile

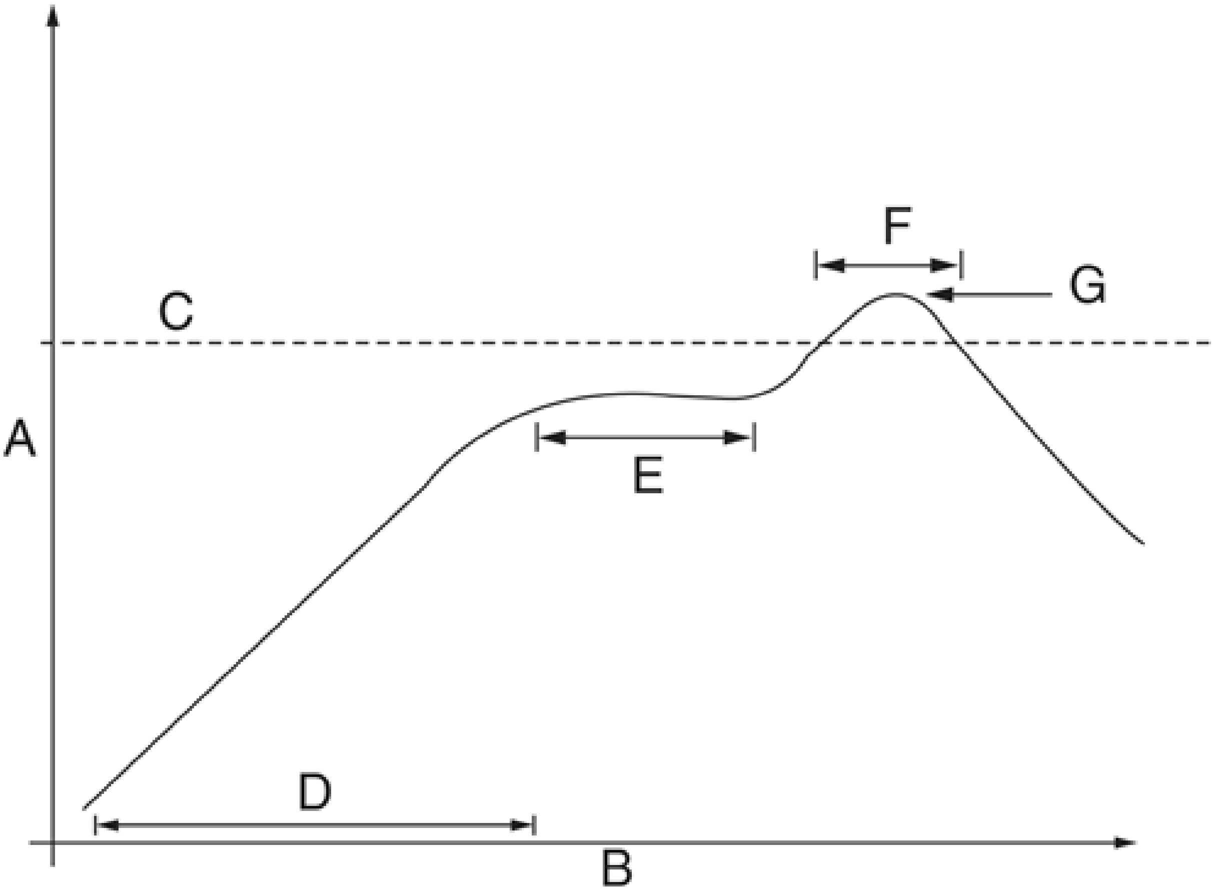


Figure 24. Thermal Profile Schematic

(1) A – Temperature.
(2) B – Time.
(3) C – Alloy liquidus temperature.
(4) D – Preheat slope = temperature ramp rate.
(5) E – Preheat dwell = soak time.
(6) F – Time above liquidus.
(7) G – Peak temperature = maximum assembly temperature.

Table 34. Reflow Profile Parameters (1) (2)

ITEM	TEMPERATURE RANGE	RAMP RATE / TIME
D, preheat zone	30°C ~ 175°C	2°C ~ 4°C per second
E, soak zone	150°C ~ 200°C	60 ~ 120 seconds
C, Alloy liquidus temperature	217°C ~ 220°C	-
F, reflow zone	230°C ~ 245°C	60 ~ 90 seconds

Table 34. Reflow Profile Parameters (1) (2) (continued)

ITEM	TEMPERATURE RANGE	RAMP RATE / TIME
G, target maximum reflow temperature	250°C	-
Absolute peak temperature (3)	260°C	-

(1) This is for Pb-free (SAC 305) paste. Different pastes require different profiles for optimum performance, so it is important to consult the paste manufacturer before developing the solder profile.

(2) It is recommended that the modules do not go through the reflow process more than one time.

(3) Exceed the absolute peak temperature for certain period, e.g. 20s might damage the device or affect the reliability.

7.3.3. Other Consideration

1. Ultrasonic cleaning process is not recommended for the modules as the process might damage the module permanently, especially for the crystal oscillator in the module.
2. Conformal coating is not allowed to this module. It will impact the reliability of the module once the coating flooded into the shield.

8. Certification

8.1. Bluetooth Qualification

8.1.1. Bluetooth Qualification Information

The module series is listed on the Bluetooth SIG website as a qualified End Product with below information in the table.

Table 35. Bluetooth Qualification Information

DID/DN	QDID AND INCLUDED DN
TBD	TBD

8.1.2. Bluetooth Qualification Process

Below Bluetooth qualification process is provided for customers when they are listing their end product referencing BDE module.

1. Go to https://launchstudio.bluetooth.com/ and log in;
2. Select **Start the Bluetooth Qualification Process with No Required Testing**;
3. Project Basics:
    a. Enter your project name, it can be the product name or the product series name;
    b. Enter QDID that the product reference, in this case the QDID is TBD.
4. Product Declaration:
    a. Select the listing date. You can select a date that you want your product listed and go public, although the qualification will complete immediately after your submission.
    b. Add every product that integrated with this module. You can add a series of individual product models that use the same design/module without any modification.
5. Declaration ID:
    a. Select a DID. If you don't have one, you need to purchase a DID for your product by clicking Pay Declaration Fee.
6. Review and Submit:
    a. Review all information that you have entered and make sure no mistakes;
    b. Tick all check boxes if you confirmed above information and add your name to the signature page;
    c. Click **Signature Confirmed – Complete Project & Submit Product(s) for Qualification**.
7. The qualification will be done immediately and your product will be listed to the Bluetooth SIG website as per your required listed date in step (4).

For more information about listing your product to Bluetooth SIG, please visit below webpage:

https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

8.2. Regulatory Compliance

8.2.1. Regulatory Compliance Information

TBD.

8.2.2. Certified Antennas

TBD.

8.2.3. FCC Compliance

TBD.

8.2.4. IC/ISED Compliance

TBD.

8.2.5. MIC/TELEC Compliance

TBD.

8.2.6. CE/ETSI Compliance

TBD.

9. Ordering Information

TBD.

10. Revision History

Table 36. Revision History

REVISION	DATE	DESCRIPTION
V0.1	20-April-2025	• Preliminary, draft
V0.2	16-May-2025	• Updated Table 2. Pinout Description, added UART2
V0.3	25-July-2025	• Removed support for 16MB flash • Added more notes in Table 2
V0.4	10-April-2026	• Updated template • Updated module design. Modified data accordingly
V0.5	24-April-2026	• Updated pin diagram • Updated pin descriptions

11. Important Notice and Disclaimer

The information contained herein is believed to be reliable. BDE makes no warranties regarding the information contain herein. BDE assumes no responsibility or liability whatsoever for any of the information contained herein. BDE assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for BDE products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.

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